CDC® CYBER 170
COMPUTER SYSTEMS

170 SYSTEMS HARDWARE HANDBOOK

CDC® CYBER 170 COMPUTER SYSTEMS

prepared by . . .

TECHNICAL PUBLICATIONS WRITING
FACILITY CODE ARH219

SYSTEMS HARDWARE HANDBOOK

PUBLICATION NO. 60447600

AUGUST 1975

REVISION RECORD

REVISION	DESCRIPTION
A	Manual released.
(8-1-75)	

Publication No.
60447600

PREFACE

The CDC® CYBER 170 Computer Systems Hardware Handbook has been prepared specifically for Control Data salesmen and pre-sales analysts. The handbook gives a broad view of the CDC CYBER 170 Computer Systems and is intended to complement information located in other CDC hardware publications listed in Section 5.

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FIGURES

TABLES

CDC CYBER 170 SERIES

The CDC CYBER 170 series is a family of software-compatible computer systems (Figure 1-1) consisting of models 172 through 175. These systems rank among the largest and most powerful computers in the world. Unique features of each of the systems contribute to a wide range of memory sizes, processing power, and input/output options to meet initial and future needs of a customer.

Models 172 and 173 are single-central-processor systems identical in architecture and operating characteristics, except that model 173 provides increased performance as the intermediate-sized system of the family. The architecture of model 174 differs from models 172 and 173 with the use of a dual central processor that increases the model 174 performance by processing programs in parallel.

The most powerful member of the CDC CYBER 170 series is the model 175. This system offers still higher performance with the use of a processor that has nine functional units to provide a high degree of overlap of instruction retrieval and execution.

In all the CDC CYBER 170 models, an extended core storage (ECS) subsystem is optional as an extension to the central memory for program and information storage. The ECS functions as a buffer between a high-speed central memory in the mainframe and low-speed mass storage equipment. Flexibility of the system includes the ability of the ECS to be shared by separate CDC CYBER 70 or 170 systems in a multimainframe environment and the ECS size which ranges from 125 thousand to 2 million 60-bit words.

The CDC CYBER 170 system capabilities are described by performance indicators such as instruction execution time, memory speed, and data transfer rates. The instruction execution time for the most powerful model of the product line is a maximum of 40 million instructions per second, based on theoretical calculation using the internal clock time of the computer.
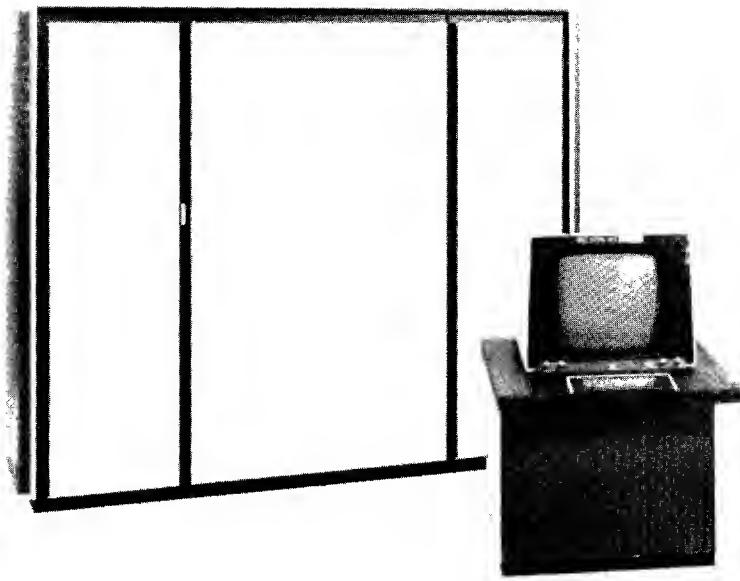
ONE-BAY

• MODEL 172

• MODEL 173
  (BASIC SYSTEM)

TWO-BAY

• MODEL 173
  (WITH MAINFRAME
  OPTIONS)

• MODEL 174
  (BASIC SYSTEM)
       OR
  (WITH MAINFRAME
  OPTIONS)

• MODEL 175
  (BASIC SYSTEM)
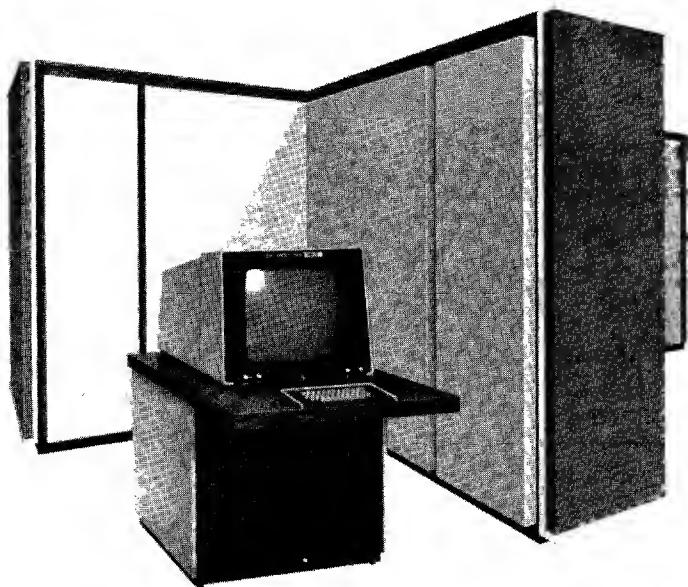
THREE-BAY

• MODEL 175
  (WITH MAINFRAME
  OPTIONS)

Figure 1-1. CDC CYBER 170 Systems

The memory speed refers to the memory cycle time, the minimum time interval between references to central memory by the central computer. Although the cycle time is 400 nanoseconds for any individual word of central memory, a bank-phasing method permits up to 8 memory banks (16 memory banks for model 175) to be referenced in parallel. This means that the effective central memory transfer rate is not limited by the memory cycle time and, consequently, a request for central memory can be issued at a maximum rate of one every 50 nanoseconds.

Transfer of data between the central memory and ECS is one 60-bit word every 100 nanoseconds. Transfer of data is carried out in blocks of data that contain up to 131 thousand 60-bit words.

The ECS input/output (I/O) maximum transfer rate is 100 million characters every second. This rate is based on no channel conflicts, ten 6-bit characters per word, and a transfer of one word every 100 nanoseconds.

HARDWARE FEATURES

The CDC CYBER 170 systems are a logical evolution of earlier produced CDC 6000 and CYBER 70 systems. Building on the design concepts of these earlier systems, Control Data now provides a broad product line application of integrated circuitry in the CDC CYBER 170 family. This circuitry covers the full range of small-scale integration (SSI), 2 to 15 logic gates per integrated circuit, medium-scale integration (MSI), 15 to 100 logic gates per integrated circuit, and large-scale integration (LSI), 100 or more logic gates per integrated circuit. The integrated circuitry of the CDC CYBER 170 family includes emitter-coupled logic (ECL) and metal-oxide semiconductor (MOS) which have been primarily responsible in reducing power, cooling, and cabinet size requirements from comparable CDC CYBER 70 systems.

Some examples of the size reductions can be shown by pointing out that a CDC CYBER 170/ Model 173 with 131K words (60 bits per word) of memory is one-third the size of a CDC CYBER 70/Model 73. A CDC CYBER 170/Model 174 with 262K words of memory is one-third the size of a CDC CYBER 70/Model 74 with only 131K words of memory. In addition, two data channel converters are built into the mainframes of the CDC CYBER 170 systems rather than in separate cabinets as in the CDC CYBER 70 systems. These size reductions result in significant reductions in floor space requirements and simplification of system installations in new and existing facilities.

Automated circuit module assembly and semiautomatic wire-wrap terminations on the main-frame back panel are other improved manufacturing techniques that have reduced manufacturing costs, assembly time, and assembly errors that are more characteristic of manual assembly. These techniques contribute to the overall attractiveness of the CDC CYBER 170 family price/performance.

In addition to using advanced technologies and assembly techniques, Control Data has improved upon the well-established and proven hardware features of the CDC CYBER 70 systems architecture. Using a CDC CYBER 70/Model 73 as a basis for comparison, models of the CDC CYBER 170 line include the following new hardware features.

- Direct Addressability of 262 Thousand 60-Bit Words

  Offers twice the capacity as the CDC CYBER 70 systems and permits the user to execute more programs in multiprogramming mode.

- Double Speed Peripheral Processors

  Permit CDC CYBER 170 Peripheral Processing Systems and related data channels to operate at the same speed or at twice the speed of CDC CYBER 70 peripheral processors and channels. This improvement provides a main benefit of connecting more and, in the future, faster I/O devices.

- Parity

  Provides for the recognition of errors on data and address paths during transfer of data and instructions.

- Single-Error Correction Double-Error Detection (SECDED)

  Provides automatic correction of single-bit memory errors and detection of multiple-bit memory errors.

- Status and Control Register

  Provides control of new hardware features without impacting existing software. The control part of the register includes such functions as logging and monitoring error information and testing of parity and SECDED networks.

- Memory Reconfiguration

  Permits a user to lock out a failing part of memory that contains multiple-bit errors and continue operation in a reconfigured mode. Memory reconfiguration allows a user to defer corrective maintenance and improve system availability.

- Force Peripheral Processor Exit

  Permits a peripheral processor to exit out of any instruction which causes the processor to hang — operate in a continuous loop.

- Forced Deadstart

  Permits individual peripheral processors to be deadstarted with the use of the status and control register.

IMPROVED PERFORMANCE

The use of new technology has greatly improved the performance of CDC CYBER 170 systems over the CDC CYBER 70 systems. Some of the reasons for the improved performance include shorter clock period, faster peripheral processor (PP) cycle time, a more powerful central processor, and an instruction word stack.

The CDC CYBER clock periods have been shortened from 100 nanoseconds in model 73 to 50 nanoseconds in models 172, 173 and 174, and 25 nanoseconds in model 175.

The cycle time of the PPs may be optionally decreased from 1000 to 500 nanoseconds. This speed change results in the possibility of increasing the speed of I/O operations.

The more powerful central processor of the model 175 is a result of using nine independent functional units that permit simultaneous arithmetic operations. An instruction word stack (IWS) in model 175 also contributes to the performance by providing rapid access to multireferenced instructions in short program loops without references to central memory for instruction retrieval.

IMPROVED RELIABILITY AND MAINTAINABILITY

The improved reliability of the CDC CYBER 170 systems over the CDC CYBER 70 systems has been accomplished by the use of state-of-the-art technology and new design features such as SECDED. SECDED allows the computer to continue reliable operation despite single bit errors that may come from central memory. The computer accomplishes this by correcting the errors through the use of SECDED code bits which accompany each word sent to and from central memory.

The improved maintainability of the CDC CYBER 170 systems over the CDC CYBER 70 systems has been accomplished by adding such features as the status and control register, parity networks, central memory reconfiguration, and instruction word stack (IWS) degradation in model 175.

The status and control register is primarily a hardware and a software maintenance tool. For hardware maintenance, the register provides programmable voltage margin variations for selected central processor modules in model 175, memory circuitry maintenance checks, isolation of memory errors to a single module, and identification of interchassis parity errors.

Parity networks add to the reliability and maintainability by flagging parity errors on all address and data trunks. When a parity error occurs, an error flag is sent to the requesting port and to the status and control register. In addition, three port code bits and four status bits are sent to the status and control register and provide a basis for locating the cause of the error.

Central memory reconfiguration is a manually controlled function that permits a failing part of central memory to be quickly bypassed to provide a continuous block of usable memory. This function enhances the system availability for the user and minimizes the system downtime due to a memory failure.

The stack degradation allows words 1 through 4 or words 1 through 10 of the 12-word stack in model 175 to be disabled in the event of a failing word. The words are quickly disabled by the use of a maintenance switch.

ADVANCED TECHNOLOGY

The advanced technology of the CDC CYBER 170 systems basically consists of using ECL integrated circuits and MOS integrated circuits. The ECL circuits are used throughout the logic modules in models 172 through 174 and on all logic modules of model 175, except in the central processor. The high-speed model 175 central processor requires components with fast switching times that are not yet available as an industry standard for integrated circuits. Consequently, the model 175 central processor uses discrete components in 7000-type modules that have proven performance in the CDC 7000 series systems. The MOS circuits are located in central and peripheral processor memories and perform the data storage that is performed by ferrite-core memories in the CDC CYBER 70 systems.

ECL INTEGRATED CIRCUITS

The ECL integrated circuit used in the CDC CYBER 170 systems is the most advanced of standard manufactured circuits available from multiple vendor sources. It is a microcircuit that contains nonsaturating logic that ranges from simple gates and flip-flops to complex circuitry for arithmetic logic functions. A highly desirable characteristic of the nonsaturating microcircuits is that the circuits avoid the lower speed limitations required by the storage time of integrated circuits which contain circuitry such as transistor-transistor logic (TTL). Some of the important technical features offered by the ECL circuits are:

- High input impedance/low output impedance permits large fanout and versatile drive characteristics.

- Minimal power supply noise generation due to differential amplifier design.

- Nearly constant power supply current drain.

- Minimal cross talk due to low-current switching on signal paths.

- Low chip power consumption; less than 8 milliwatts in some complex function chips.

- No line drivers needed due to open emitter outputs of ECL.

- Capability of driving twisted-pair transmission lines up to 1000 feet.

- Simultaneous complementary outputs available at logic element outputs without external inverters.

MOS INTEGRATED CIRCUITS

The MOS integrated circuits are silicone microcircuits with capacitive characteristics that make them suitable as high density storage devices. Manufacturing techniques and operating characteristics of the MOS circuits give them a number of advantages over the ferrite-core memories. These advantages apply also to ECL circuits in comparison to discrete components.

- Lower cost

- Faster operation, on a system basis

- Lower power requirements

- Higher reliability

- Higher densities, as low as one-seventh the space of core memories

A characteristic of the MOS circuits is that they are unipolar, unlike the more common junction transistors which are bipolar. The unipolar semiconductors use either holes (p-type) or electrons (n-type) as carriers of electronic charge but not both. The bipolar semiconductors use the holes and electrons. The central and peripheral processor memories of the CDC CYBER 170 systems use the p-type MOS circuits.

The MOS circuits are each capable of storing 1024 bits. Twenty of the circuits are arranged (four columns by five rows) on each of the computer's memory modules, giving each module a high-density storage capacity of 20,480 bits. Any of the bits in any of the central memory MOS circuits is randomly accessible, making central memory a random access memory.

Because the MOS circuits permit assembly of memory in small modules, maintainability of the computer central memories is easier than for memories that use the more difficult-to-replace ferrite cores. The physical organization of central memory and the SECDED feature permits identification of memory problems on a module level and consequently, allows for quick replacement of bad memory sections. The memory modules also require a lower inventory level for replacement purposes.

PROVEN ARCHITECTURE

The basic architecture (Figure 1-2) of the CDC CYBER 170 systems is the same as the CDC CYBER 70 systems. This architecture is based on the central processor (CP), dedicating its time to execution of user-written code and letting other components within the system processing hierarchy perform operating system functions for I/O monitoring which do not need a high-power CP instruction set. Each processing level, therefore, performs in the most effective manner. This type architecture provides a unique concept called distributive processing. Distributive processing offers the system users the most cost-effective computing capabilities and allows them to use those capabilities in parallel. The result is high execution speed combined with a high total-system throughput. The system also offers a similar hierarchy of storage capability.

Figure 1-3 shows the basic hardware of the nondistributive and distributive processing systems. The nondistributive processing system is a conventional computer system with one level of computing at the CP. This system has direct I/O channel communications with the CP and places nearly all of the processing load on the CP, burdening it with time-consuming I/O and monitoring operations.
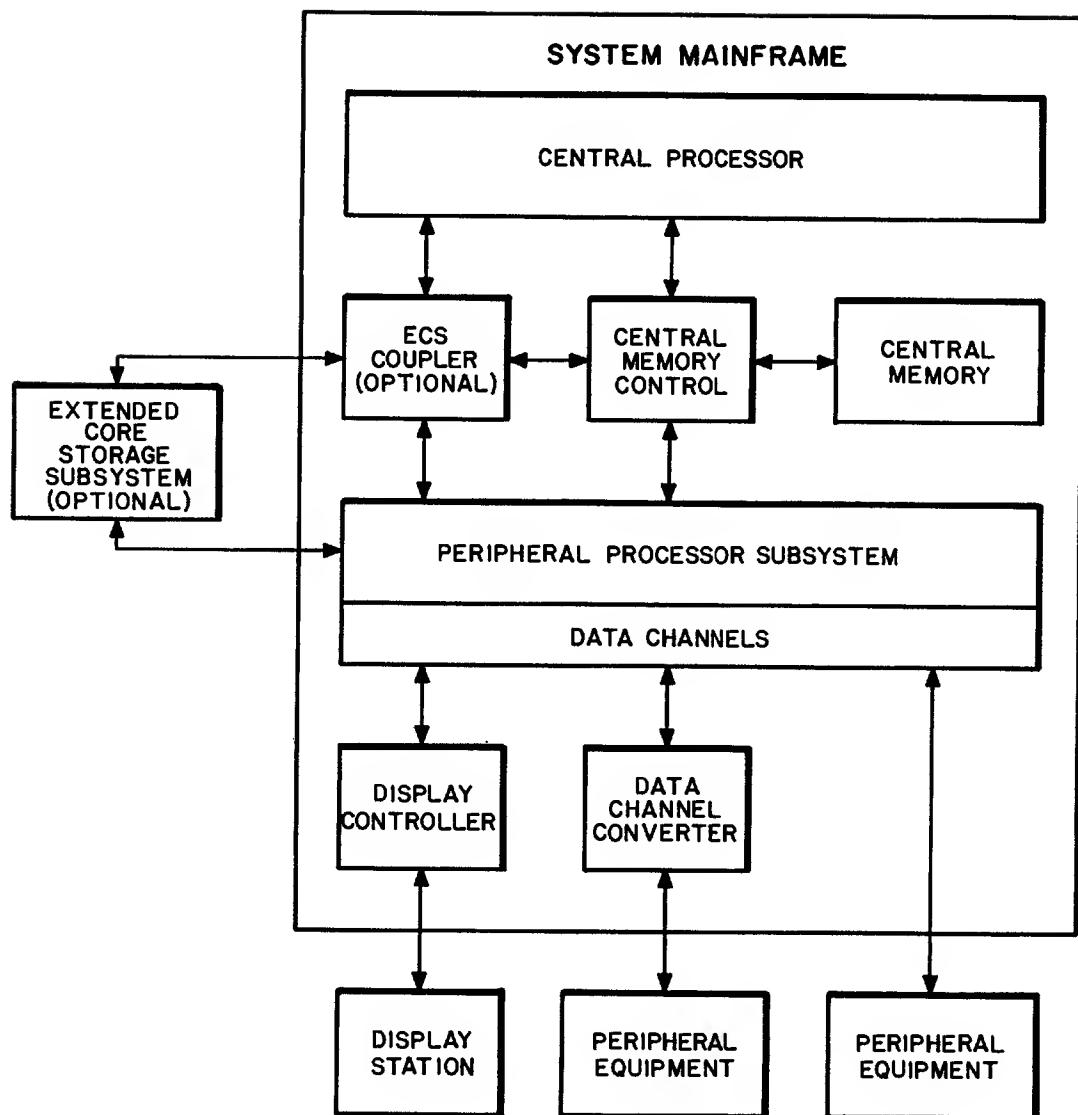
Figure 1-2. CDC CYBER 170 System Basic Architectural Configuration

NONDISTRIBUTIVE PROCESSING SYSTEM

DISTRIBUTIVE PROCESSING SYSTEM
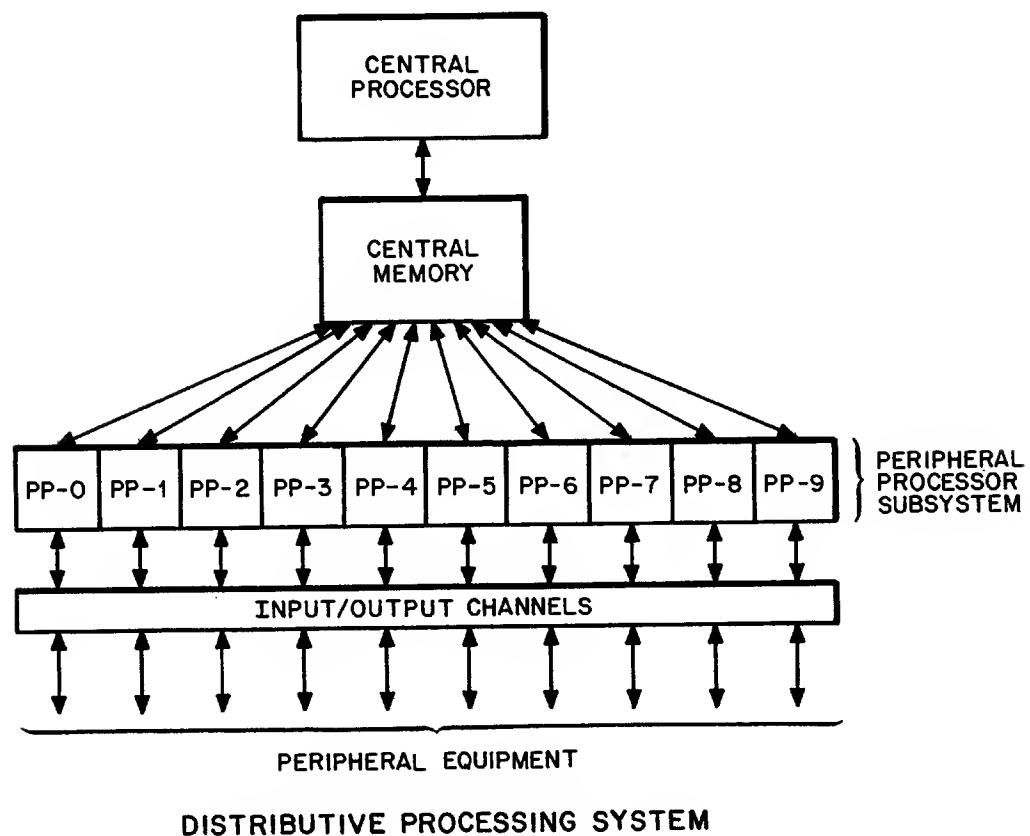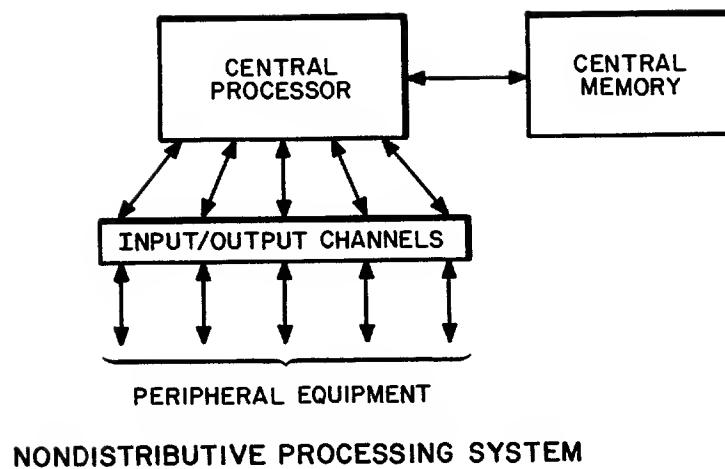
Figure 1-3.   Nondistributive and Distributive Processing Systems Hardware

The CDC interpretation of a distributive processing system includes two processing levels. A higher level processing is at the CP and a lower level processing is at a peripheral processor subsystem (PPS). The PPS may contain 10 or more individual PPs that carry out all of the computer I/O operations. Each of the PPs communicate to the CP through the central memory, completely relieving the CP from all I/O operations.

Figure 1-4 shows the advantage of the CDC CYBER 170 system (distributive processing) over a conventional system (nondistributive processing). The figure shows an example of three user programs (A, B, and C) executed in the conventional system and the same three programs executed in the CDC CYBER 170 system. In addition to executing the user programs, the central processor of the conventional system must execute the operating system programs. Consequently, only 40 to 60 percent of the CP computing time is available for the user programs. In contrast, the CP of the CDC CYBER 170 system is not burdened by the operating system. The operating system is executed by the PPS, leaving almost all of the CP computing time for the user programs. Figure 1-4 clearly shows that the CDC CYBER 170 system processes the same programs more quickly than a conventional computer system with equivalent CP power, resulting in better throughput times.

The higher throughput capability of a CDC CYBER 170 system is made possible by the PPS. The PPS provides the higher throughput by permitting the CP to use the equivalent I/O time of the conventional system as additional computing time. The 10 (up to 20 in an upgraded Model 173, 174, or 175) PPs operate in parallel to the user programs and to each other. Each PP is independent of the other and has a 4 thousand 12-bit word memory. The PPs communicate with the CP and 12 I/O channels, optionally expandable to 24 channels in an upgraded PP subsystem. Each PP is capable of executing an instruction repertoire that is optimized for I/O operations and system monitoring activities.

CONVENTIONAL SYSTEM

(NONDISTRIBUTIVE PROCESSING)

OPERATING SYSTEM UTILIZES 40 TO 60% OF CENTRAL PROCESSOR TIME.

OPERATING SYSTEM

PROGRAM A
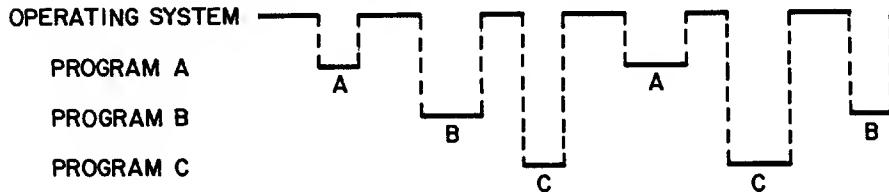
PROGRAM B

PROGRAM C

CDC CYBER 170 SYSTEM

(DISTRIBUTIVE PROCESSING)

ALMOST ALL OF CENTRAL PROCESSOR TIME IS AVAILABLE FOR PROGRAM EXECUTION
PROVIDING INCREASED THROUGHPUT TIME.

PROGRAM A
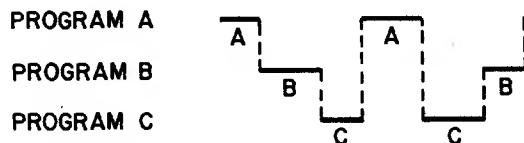
PROGRAM B

PROGRAM C

PERIPHERAL
PROCESSOR (PP)
SUBSYSTEM
UTILIZATION

.PPs PROVIDE OPERATING SYSTEM EXECUTION IN PARALLEL
WITH PROGRAM EXECUTION. PPs ALSO PROVIDE PARALLEL
EXECUTION OF OPERATING SYSTEM FUNCTIONS.

PP-0 — MONITOR

PP-1 — DISPLAY STATION

PP-2 — DISK

PP-3 — TAPE

•
•
•

PP-9 — RECORD I/O

TIME UTILIZATION BASE ⟶
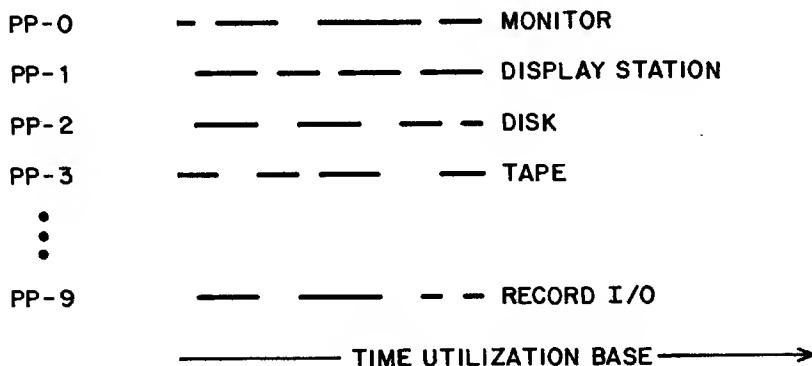
Figure 1-4. Conventional and CDC CYBER 170 Systems

BASIC SYSTEMS

The CDC CYBER 170-Series Computer Systems are functionally similar in a number of ways. The similarities are shown by a summary of the functional components for each system in Table 2-1 and by individual system block diagrams in Figures 2-1 through 2-4. In some of the systems, functional components such as the central processor (CP), central storage unit (CSU), and the peripheral processor subsystem (PPS) are duplicated. Each such duplication increases the system computing capabilities and, depending on the system model, is either part of the basic system or may be added as an option or future upgrade (refer to Section 3 — System Upgrades).

In addition to the functional components within the mainframe, each computer system includes a display station and condensing unit. The display station is a separate piece of peripheral equipment and is described later in this section. The one or more condensing units for models 172 through 174 are internally mounted in the mainframes. For model 175, a single condensing unit comes as a separate unit. This unit and the internally mounted condensing units are also described later in this section.

A wide range of peripheral equipment is available for each system according to the specific needs of the user (refer to Section 4 — Peripheral Equipment Configurations).

TABLE 2-1. CDC CYBER 170 SYSTEM COMPONENTS

Components	Models			
	172	173	174	175
Mainframe:				
Central processor-0	x	x	x	-
Central processor-1	-	-	x	-
Central memory control	x	x	x	-
Central processor (includes central memory control)	-	-	-	x
Central memory, central storage unit-0	x	x	x	x
Central memory, central storage unit-1	-	*	*	x
Peripheral processor subsystem-0	x	x	x	x
Peripheral processor subsystem-1	-	*	*	*
Two data channel converters for peripheral processor subsystem-0	x	x	x	x
Two data channel converters for peripheral processor subsystem-1	-	*	*	*
Display controller	x	x	x	x
Extended core storage coupler	*	*	*	*
One 3-ton internally mounted condensing unit	x	x	-	-
Two 3-ton internally mounted condensing unit	-	*	x	-
One 10-ton externally mounted condensing unit	-	-	-	x
Display station (first)	x	x	x	x
Display station (second)	*	*	*	*
Extended core storage subsystem	*	*	*	*

x = Standard

- = Not available

* = Optional

CENTRAL PROCESSOR

| LARGE ARITHMETIC SECTION | SMALL ARITHMETIC SECTION |
| INSTRUCTION CONTROL | |

ECS COUPLER ①

CENTRAL MEMORY CONTROL

CENTRAL MEMORY ②

CENTRAL STORAGE UNIT

ECS MEMORY BANKS

ECS CONTROLLER ③

EXTENDED CORE STORAGE SUBSYSTEM ①

DISTRIBUTIVE DATA PATH ④

DISPLAY STATION

DISPLAY CONTROLLER

PERIPHERAL PROCESSOR SUBSYSTEM

3AR11A

TWO DATA CHAN CONVERTERS ⑤

TWO I/O CHANNELS

⑥

TEN I/O CHANNELS
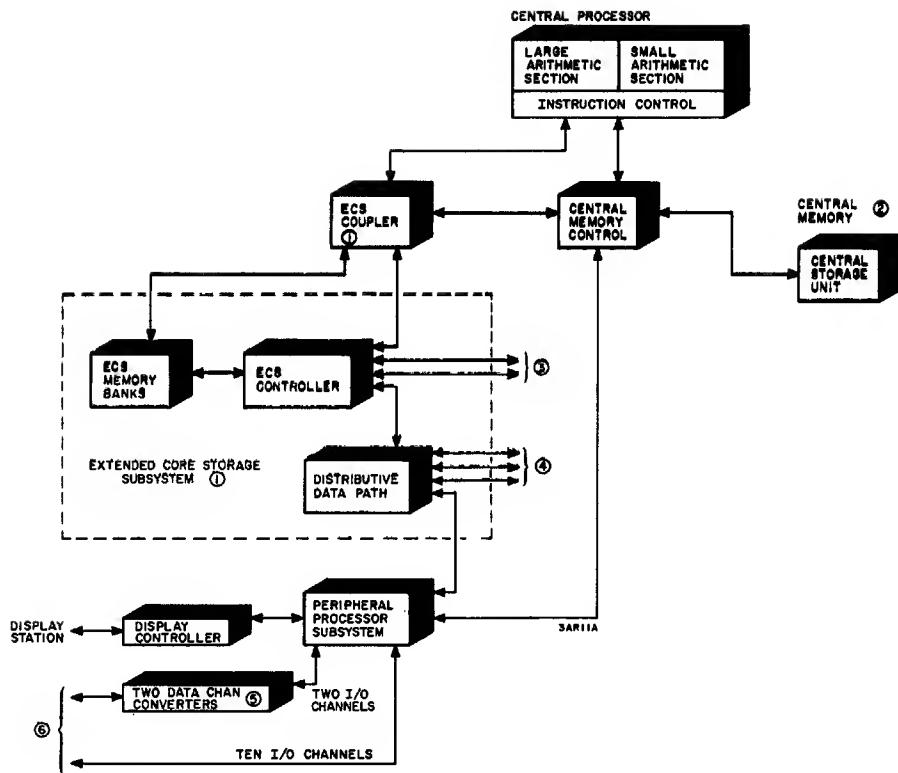
NOTES:

① OPTIONAL EQUIPMENT.

② BASIC CM CONTAINS 32,768 60-BIT WORDS. CM IS EXPANDABLE TO 49,152; 65,536; 98,304; AND 131,072 60-BIT WORDS.

③ TWO PORTS AVAILABLE FOR USE BY OTHER SYSTEMS.

④ THREE PORTS AVAILABLE AS OPTIONS FOR USE BY OTHER SYSTEMS.

⑤ TWO DATA CHANNEL CONVERTERS ARE INCLUDED IN BASIC AND OPTIONAL PP SUBSYSTEMS. ADDITIONAL CONVERTERS MAY BE ADDED EXTERNALLY.

⑥ PERIPHERAL EQUIPMENT.

Figure 2-1.   Model 172 Basic Computer System
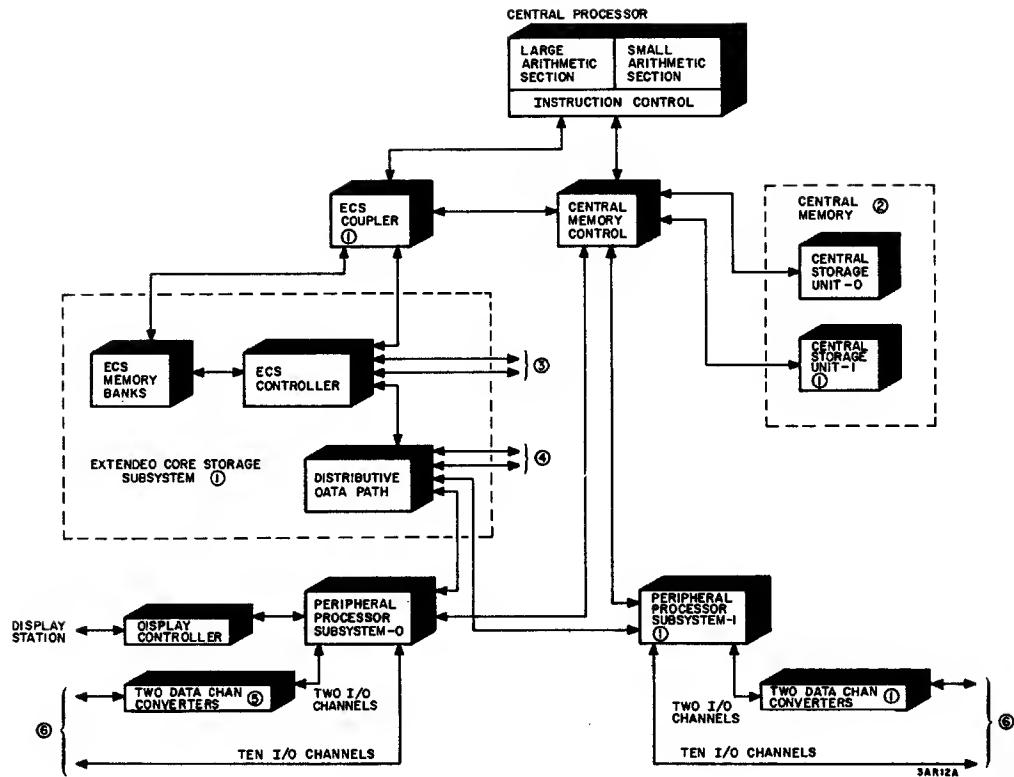
NOTES:

(1) OPTIONAL EQUIPMENT.

(2) BASIC CM CONTAINS 65,536 60-BIT WORDS. CM IS EXPANDABLE TO 98,304; 131,072; 196,608; AND 262,144 60-BIT WORDS.

(3) TWO PORTS AVAILABLE FOR USE BY OTHER SYSTEMS.

(4) TWO PORTS AVAILABLE AS OPTIONS FOR USE BY OTHER SYSTEMS.

(5) TWO DATA CHANNEL CONVERTERS ARE INCLUDED IN BASIC AND OPTIONAL PP SUBSYSTEMS. ADDITIONAL CONVERTERS MAY BE ADDED EXTERNALLY.

(6) PERIPHERAL EQUIPMENT.

Figure 2-2. Model 173 Basic Computer System
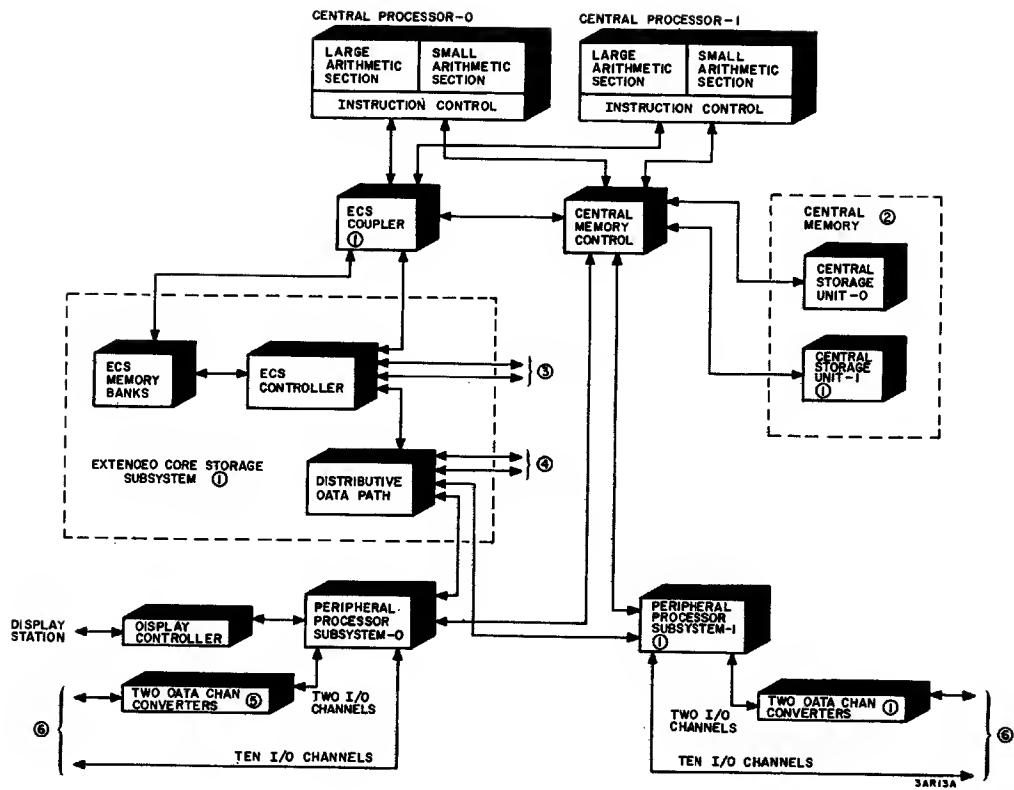
CENTRAL PROCESSOR-0   CENTRAL PROCESSOR-1

LARGE ARITHMETIC SECTION   SMALL ARITHMETIC SECTION

INSTRUCTION CONTROL

ECS COUPLER ①

CENTRAL MEMORY CONTROL

CENTRAL MEMORY ②

CENTRAL STORAGE UNIT-0

CENTRAL STORAGE UNIT-1 ①

ECS MEMORY BANKS

ECS CONTROLLER

EXTENDED CORE STORAGE SUBSYSTEM ①

DISTRIBUTIVE DATA PATH

DISPLAY STATION

DISPLAY CONTROLLER

PERIPHERAL PROCESSOR SUBSYSTEM-0

PERIPHERAL PROCESSOR SUBSYSTEM-1 ①

TWO DATA CHAN CONVERTERS ⑤

TWO I/O CHANNELS

TWO I/O CHANNELS

TWO DATA CHAN CONVERTERS ①

TEN I/O CHANNELS   TEN I/O CHANNELS

③ ④ ⑥

3AR13A

NOTES:

① OPTIONAL EQUIPMENT.

② BASIC CM CONTAINS 65,536 60-BIT WORDS. CM IS EXPANDABLE TO 98,304; 131,072; 196,608; AND 262,144 60-BIT WORDS.

③ TWO PORTS AVAILABLE FOR USE BY OTHER SYSTEMS.

④ TWO PORTS AVAILABLE AS OPTIONS FOR USE BY OTHER SYSTEMS.

⑤ TWO DATA CHANNEL CONVERTERS ARE INCLUDED IN BASIC AND OPTIONAL PP SUBSYSTEMS. ADDITIONAL CONVERTERS MAY BE ADDED EXTERNALLY.

⑥ PERIPHERAL EQUIPMENT.

Figure 2-3. Model 174 Basic Computer System

NOTES:

① OPTIONAL EQUIPMENT.

② BASIC CM CONTAINS 65,536 60-BIT WORDS. CM IS EXPANDABLE TO 98,304; 131,072; 196,608; AND 262,144 60-BIT WORDS.

③ TWO PORTS AVAILABLE FOR USE BY OTHER SYSTEMS.

④ TWO PORTS AVAILABLE AS OPTIONS FOR USE BY OTHER SYSTEMS.

⑤ TWO DATA CHANNEL CONVERTERS ARE INCLUDED IN BASIC AND OPTIONAL PP SUBSYSTEMS. ADDITIONAL CONVERTERS MAY BE ADDED EXTERNALLY.

⑥ PERIPHERAL EQUIPMENT.

Figure 2-4. Model 175 Basic Computer System

SYSTEM MAINFRAMES

The CDC CYBER 170 system mainframes have chassis configurations (Figures 2-5 through 2-8) that differ according to their model numbers and optional units. The basic mainframes contain functional components that consist of: a central processor unit (CPU) or CP, central memory control (CMC), central memory (CM), PPS, data channel converters, and a display controller. The following paragraphs describe the functional components and Tables 2-2 through 2-5 provide system comparisons of the functional characteristics.

CENTRAL PROCESSOR — MODELS 172 THROUGH 174

The CP consists of large and small arithmetic sections and an instruction control section. The arithmetic sections perform arithmetic operations by manipulation of 18- and 60-bit operands. The instruction control section directs the arithmetic operations, directs character manipulative functions of compare/move instructions, and interfaces the CMC and arithmetic sections.

ARITHMETIC SECTIONS

The large and small arithmetic sections form a unified arithmetic unit. Instructions use the large section of the unit for 60-bit operand manipulation and the small section for 18-bit operand manipulation. The large arithmetic section contains a 108-bit adder, shift network, normalize network, and shift counter. Instructions use the small arithmetic section for the manipulation of 18-bit operands and for exponent manipulation. The small arithmetic section contains an 18-bit adder. The arithmetic sections also provide other arithmetic functions required by the CP for instruction execution.

INSTRUCTION CONTROL SECTION

The instruction control section consists of 24 operating registers, 7 support registers, and instruction control logic.

The following operating and support register descriptions also apply to the model 175 CP and are, therefore, not repeated in that CP description.
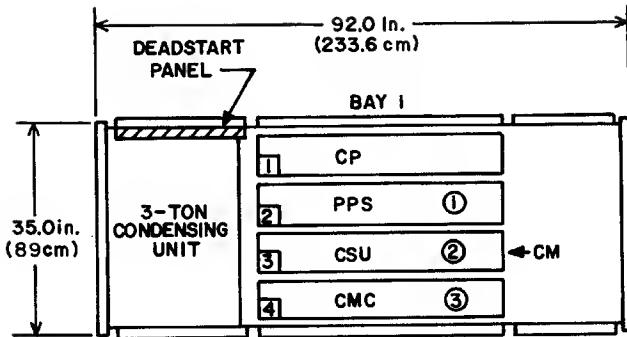
NOTES:

① CHASSIS 2 ALSO CONTAINS TWO DATA CHANNEL CONVERTERS AND A DISPLAY CONTROLLER.

② CSU IS EXPANDABLE FROM 32,768 TO 49,152; 65,536; 98,304; AND 131,072 WORDS.

③ WHEN ECS IS USED, CHASSIS 4 ALSO CONTAINS THE ECS COUPLER.

Figure 2-5. Model 172 Chassis Configuration (Top Cutaway View)
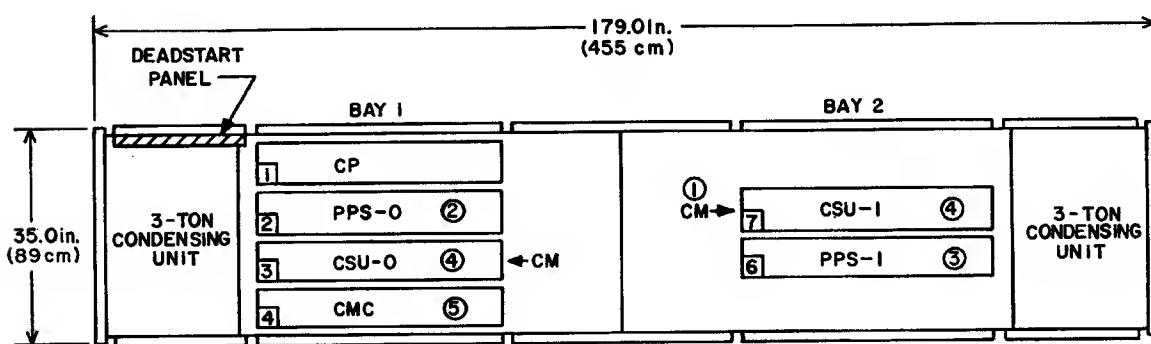
NOTES:

① BAY 2 AND CHASSIS 6 AND 7 OPTIONAL.

② CHASSIS 2 ALSO CONTAINS TWO DATA CHANNEL CONVERTERS AND A DISPLAY CONTROLLER.

③ CHASSIS 6 MAY CONTAIN TWO OPTIONAL DATA CHANNEL CONVERTERS.

④ CSU-0 IS EXPANDABLE FROM 65,536 TO 98,304 AND 131,072 60-BIT WORDS. CSU-1 IS OPTIONAL AND EXPANDABLE LIKE CSU-0. CSU-0 AND CSU-1 PROVIDE UP TO 262,144 60-BIT WORDS.

⑤ WHEN ECS IS USED, CHASSIS 4 ALSO CONTAINS THE ECS COUPLER.

Figure 2-6. Model 173 Chassis Configuration (Top Cutaway View)
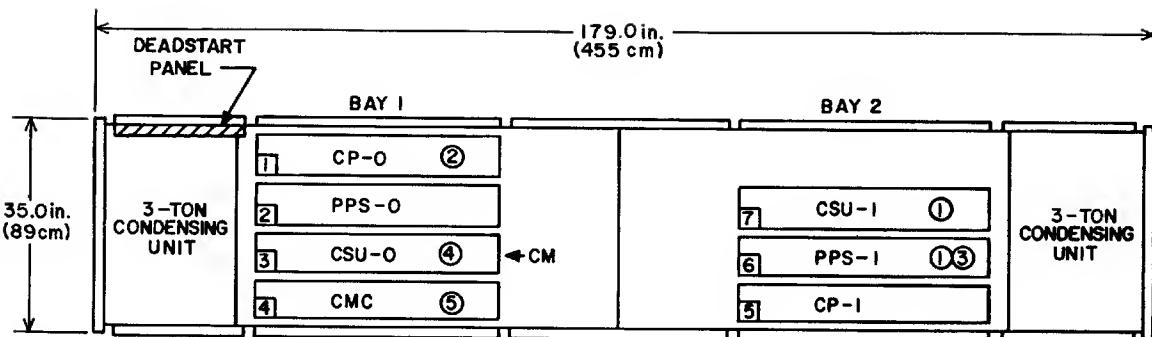
NOTES:

① BAY 2 AND CHASSIS 6 AND 7 ARE OPTIONAL.

② CHASSIS 2 ALSO CONTAINS TWO DATA CHANNEL CONVERTERS AND A DISPLAY CONTROLLER.

③ CHASSIS 6 MAY CONTAIN TWO OPTIONAL DATA CHANNEL CONVERTERS.

④ CSU-0 IS EXPANDABLE FROM 65,536 TO 98,304 AND 131,072 60-BIT WORDS. CSU-1 IS OPTIONAL AND EXPANDABLE LIKE CSU-0. CSU-0 AND CSU-1 PROVIDE UP TO 262,144 60-BIT WORDS.

⑤ WHEN ECS IS USED, CHASSIS 4 ALSO CONTAINS THE ECS COUPLER.

Figure 2-7.   Model 174 Chassis Configuration (Top Cutaway View)
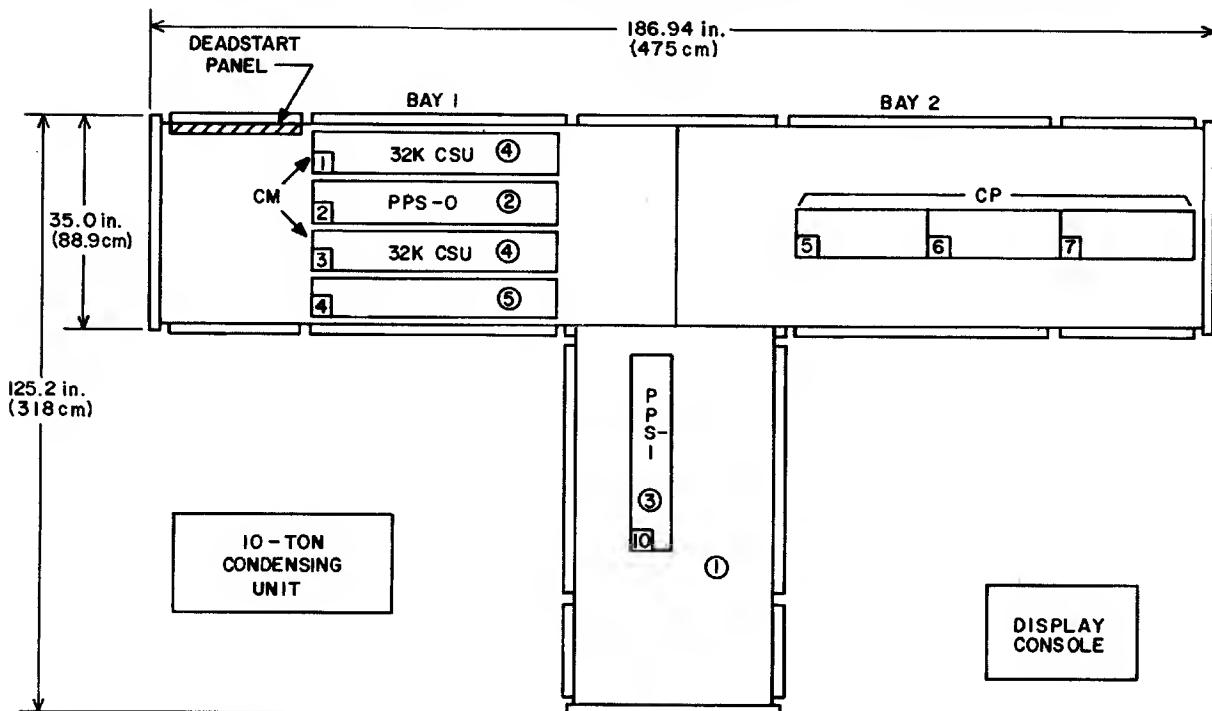
NOTES:

① BAY 3 AND CHASSIS 10 ARE OPTIONAL.

② CHASSIS 2 ALSO CONTAINS TWO DATA CHANNEL CONVERTERS AND A DISPLAY CONTROLLER.

③ CHASSIS 10 MAY CONTAIN TWO OPTIONAL DATA CHANNEL CONVERTERS.

④ CSU CHASSIS ARE EXPANDABLE FROM 65,536 TO 98,304; 131,072; 196,608; 262,144 60-BIT WORDS.

⑤ WHEN ECS IS USED, CHASSIS 4 CONTAINS THE ECS COUPLER.

Figure 2-8.   Model 175 Chassis Configuration (Top Cutaway View)

TABLE 2-2. CENTRAL PROCESSOR FUNCTIONAL CHARACTERISTICS

Functional Characteristics	Models			
	172	173	174	175
60-bit internal word	x	x	x	x
Computation in fixed- and floating-point arithmetic	x	x	x	x
Eight 60-bit operand X registers	x	x	x	x
Eight 18-bit address A registers	x	x	x	x
Eight 18-bit index B registers	x	x	x	x
Character manipulation by compare/move instructions	x	x	x	-
Synchronous internal logic with 50-nanosecond clock period	x	x	x	-
Large and small arithmetic sections	x	x	x	-
Synchronous internal logic with 25-nanosecond clock period	-	-	-	x
12-word instruction word stack	-	-	-	x
Nine functional units	-	-	-	x

x = Standard
- = Not available

TABLE 2-3. CENTRAL MEMORY FUNCTIONAL CHARACTERISTICS

Functional Characteristics	Models			
	172	173	174	175
Cycle time of 400 nanoseconds	x	x	x	x
Maximum transfer rate of one word each 50 nanoseconds	x	x	x	x
Semiconductor memory of 32,768 words (60-bit words plus 8 error detection/correction bits per word)	x	-	-	-
Expandable to 49,152; 65,536; 98,304; and 131,072 words	*	-	-	-
Semiconductor memory of 65,536 words (60-bit words plus 8 error detection/correction bits per word)	-	x	x	x
Expandable to 98,304; 131,072; 196,608; and 262,144 words	-	*	*	*
Organized into eight independent banks per CSU	x	x	x	-
Organized into 16 independent banks throughout CSU-0 and CSU-1	-	-	-	x

x = Standard
- = Not available
* = Optional

TABLE 2-4. PERIPHERAL PROCESSOR SUBSYSTEM
FUNCTIONAL CHARACTERISTICS

Functional Characteristics	Models			
	172	173	174	175
12-bit internal word	x	x	x	x
Binary computation in fixed-point arithmetic	x	x	x	x
Selectable operating speeds of 1X or 2X (1X equals major cycle of 1000 nanoseconds and minor cycle of 100 nanoseconds; 2X equals major cycle of 500 nanoseconds and minor cycle of 50 nanoseconds)	x	x	x	x
10 PPs time-share access to CM	x	x	x	x
Each PP has internal semiconductor memory of 4096 words (12-bit words plus 1 parity bit per word, odd parity)	x	x	x	x
Twelve I/O channels, each accessible by any of the PPs	x	x	x	x
Status and control register	x	x	x	x
Real-time clock	x	x	x	x
Each I/O channel carries 12-bit words plus 1 parity bit per word (odd parity)	x	x	x	x
Expandable to 20 PPs and 24 I/O channels	-	*	*	*

x = Standard
- = Not available
* = Optional

TABLE 2-5. DATA AND ADDRESS CHECKING
FUNCTIONAL CHARACTERISTICS

Functional Characteristics	Models			
	172	173	174	175
Parity check data between CP-0 and CMC	x	x	x	-
Parity check data between CP-1 and CMC	-	-	x	-
Parity check data between PPS-0 and CMC	x	x	x	x
Parity check data between PPS-1 and CMC	-	x	x	x
Parity check data between ECS and CMC	x	x	x	x
Single-error correction double-error detection (SECDED) between CM and CMC	x	x	x	x
Parity check address from CP-0 to CMC	x	x	x	-
Parity check address from CP-1 to CMC	-	-	x	-
Parity check address from PPS-0 to CMC	x	x	x	x
Parity check address from PPS-1 to CMC	-	x	x	x
Parity check address from CMC to CM	x	x	x	x
Parity check data between CM and CMC (non-SECDED mode only)	x	x	x	x
Parity check on PPS memory data	x	x	x	x

x = Standard
- = Not available

Operating Registers

The operating registers consist of X, A, and B registers. These registers provide the basic function of minimizing memory references for arithmetic operands and results.

Eight 60-bit operand X registers (X0 through X7) are the principal data handling registers for computation. Data flows from these registers to CM. Data also flows from CM into these registers. All 60-bit operands involved in computation must originate and terminate in these registers.

Eight 18-bit A registers (A0 through A7) are essentially CM operand address registers associated one-for-one with the X registers. Placing a quantity into an address register (A1 through A5) causes an immediate CM read reference to that relative address and sends the CM word to the corresponding operand register (X1 through X5). Similarly, placing a quantity into address register A6 or A7 causes the word in the corresponding X6 or X7 operand register to be written into that relative address of CM.

Eight 18-bit index B registers (B0 through B7) are primarily indexing registers for controlling program execution. Program loop counts may be incremented or decremented in these registers.

Support Registers

Seven support registers are used to assist the operating registers during the execution of programs. The support registers are loaded from CM during an exchange sequence. With the exception of the program address (P) register, the contents of the support registers cannot be altered during the execution interval of an exchange package. When the execution interval has been completed, the data in the support registers is sent back to CM.

Instruction Control

The instruction control logic performs instruction translation and control sequences. Each control sequence obtains the necessary instruction operands from the operating registers and provides the control signals for execution. Instructions read from CM are 60-bit instruction words that are in four 15-bit groups, two 30-bit groups, or a combination of 15-bit and 30-bit groups. The 15-bit groups are termed parcels with the first parcel (parcel 0) being

the highest-order 15 bits of a 60-bit CM word. Second, third, and fourth parcels (parcels 1, 2, and 3) follow in order. The 30-bit groups contain two 15-bit parcels.

CENTRAL PROCESSOR — MODEL 175

The CP consists of a CPU, nine functional units, and a CMC. The CPU, together with the functional units, executes programs stored in CM. The CMC controls all CM accesses.

The CMC of model 175 is located within the CP chassis of bay 2, unlike the CMCs of models 172 through 174 which are located in individual chassis of bay 1. Although the physical locations of the CMCs of some models differ, the CMC functions of all models are similar and are, therefore, described together under Central Memory Control in this section.

CENTRAL PROCESSING UNIT

The CPU consists of 24 operating registers, 7 support registers, and instruction control. The CPU includes the registers and control logic to direct the arithmetic operations and provide interface between the functional units and CMC. In addition to instruction execution, the CPU performs instruction fetching, address preparation, memory protection, and data fetching and storing. Figure 2-9 illustrates the general flow of information.

The CPU reads 60-bit words from CM and enters them in the instruction word stack (IWS) which is capable of holding up to twelve 60-bit words. Each instruction word, in turn, leaves the IWS and enters the current instruction word (CIW) register for interpretation and testing. The CIW register holds four 15-bit instructions, two 30-bit instructions, or combinations of the two types of instructions. The 15- or 30-bit instructions issue individually from the CIW register. The functional units obtain the instruction operands from and store results in 24 operating registers. Reservation control keeps an account of active operating registers to resolve conflicts.
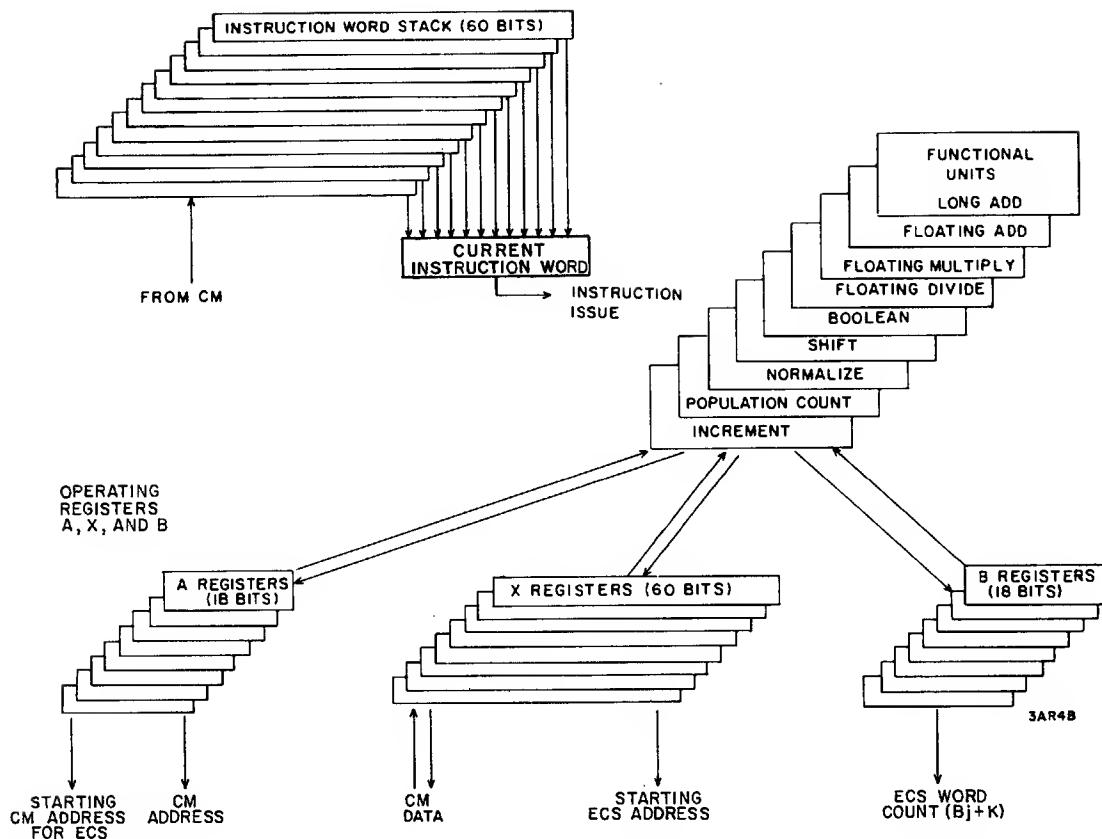
Figure 2-9. Model 175 CPU Information Flow

Operating Registers

The operating registers consist of eight X registers, eight A registers, and eight B registers.
The registers function as described for models 172 through 174.

Support Registers

The support registers include seven registers that are used to assist the operating registers
during the execution of programs. The support registers function as described for models
172 through 174.

Instruction Control

The main instruction control components include an IWS, instruction address stack (IAS),
CIW, and P register. The instruction control reads 60-bit instruction words from CM and

issues them in 15-, 30-, or 60-bit instruction groups to the CP functional units for execution. The instruction control also performs instruction translation and control of the exchange, ECS block copy, normal jump, and return jump sequences.

Instruction Word Stack

The IWS is a group of twelve 60-bit registers that holds program instruction words for execution. It is essentially a moving window in the program code. The IWS is filled two words ahead of the program address currently being executed. A program loop of up to 10 instruction words may be entirely contained within the IWS. When this happens, the instruction loop may be executed repeatedly without further references to CM. When an instruction causes a jump out of stack, the stack is voided. Voiding the stack means that the IWS is not accessible, and the IAS is cleared. New instructions must then be read from CM into the IWS and the IAS.

The 12 IWS registers are individually identified by rank. The rank 1 register contains the oldest data. If the IWS contains sequential program instruction words, the content of the rank 1 register corresponds to the lowest CM address in the IAS.

The IWS is shifted to accommodate a new word arriving from CM. New information arriving from CM is entered in rank 12. Ranks 11 through 1 are cleared and entered with information from the next highest-order rank. The information in rank 1 is discarded.

Instruction Address Stack

The IAS is a group of twelve 18-bit address registers associated with the IWS. It holds relative CM program addresses on a one-for-one basis with the program words in the IWS. The rank 1 register contains the CM address from which the word in rank 1 of the IWS is read. All ranks are compared with the current program address. If coincidence occurs for a rank, the corresponding rank in the IWS is sent to the 60-bit CIW register.

A maintenance switch is provided to disable either IAS ranks 1 through 10 or ranks 1 through 4.

Current Instruction Word Register

The CIW register is divided into four 15-bit parcels. All four parcels are loaded when an instruction word is read from the IWS. An instruction issues from the CIW register when conditions in the functional units and operating registers are such that the instruction is executed without conflicting with previously issued instructions. The other parcels are then left-shifted in the CIW register by either 15 or 30 bits, depending on the instruction format.

Program Address Register

The 18-bit P register contains the current program execution address. The register serves as a program address counter and holds the relative CM address for each program step. Since the P register is advanced one address ahead of the instruction in progress, a P buffer register holds the current program execution address. This buffered address is used for the PPS read program instruction. The content of the P register advances to the next program step as follows:

1. The P register is advanced by one when an instruction word is sent to the CIW register.

2. The P register is set to the address specified by a branch instruction. If the instruction is a return jump, the current P plus 1 is stored before entering P with the new value to allow a return to the original sequence.

3. The P register is set to the address specified in the exchange package.

Functional Units

Each of the nine functional units in the CP is a specialized arithmetic unit with algorithms for a portion of the CP instructions. Each unit is independent of the other units, and a number of functional units may be in operation at the same time. No visible registers are in the functional units from a programming standpoint. A functional unit receives one or two operands from operating registers at the beginning of instruction execution, and delivers the result to the operating registers when the function has been performed. No information is retained in a functional unit for reference in subsequent instructions.

All functional units, with the exception of the floating-multiply and -divide units, have a 1-clock-period segmentation. This means that the information arriving at a unit, or moving within a unit, is captured and held in a new set of registers every clock period. Therefore, it is possible to start a new set of operands for unrelated computation in a functional unit each clock period even though the unit may require more than 1 clock period to complete the calculation. This process may be compared to a delay line in which data moves through the unit in segments to arrive at the destination in the proper order but at a later time. All functional units perform their algorithms in a fixed amount of time. No delays are possible once the instruction has issued.

The floating-multiply unit has a 2-clock-period segmentation. Operands may enter the multiply unit in any clock period providing there was no multiply instruction initiated in the preceding clock period. There is a 1-clock-period delay in initiating a multiply instruction if another multiply instruction has just started.

The floating-divide unit is the only functional unit in which an iterative algorithm is executed. There is no segmentation possible in this unit, although the beginning of a new operation can overlap the completion of the previous operation by 2 clock periods.

The primary purpose of using functional units is to further increase the processing speed of the CP. Similar functional units are available in the CDC 6600 and CYBER 70/Model 74 systems. The units in these systems, however, are not segmented. To take full advantage of the parallel execution capabilities, optimization in the use of object codes in those systems is required to avoid unnecessary waiting for functional units to be free. The segmented functional units of the CDC CYBER 170 systems also provide the parallel execution capabilities but do not require the optimization of object codes.

CENTRAL MEMORY CONTROL

The CMC provides for the orderly flow of data between CM and the requesting elements of the system. The CMC assigns priority to CM requests, resolves bank conflicts, controls read/write operations, increments addresses, parity checks addresses and data, and generates parity for addresses and data.

CMC also has a single-error correction double-error detection (SECDED) feature. This feature allows computer operation to continue despite a single-bit failure from central memory. Two or more data-bit failures from central memory cause the program to stop and the system user is informed of the error. The user can then decide to rerun or to continue the job that caused the error. In such cases, information from associated SECDED codes makes it possible for maintenance personnel to readily correct the trouble by interpreting the SECDED codes and isolating the cause of the failure to a module level.

CENTRAL MEMORY

Each model of the computer systems has basic and optional CM sizes. The CM sizes are determined by the number of 68-bit words, 60 data bits and 8 SECDED bits, that the CMs store (refer to Tables 2-6 and 2-7). The basic CM size for each system is the smallest size listed for that system. The optional sizes are the next four larger sizes.

A CM consists of CSU-0 and CSU-1, depending on model and CM options. Each CSU contains eight CM banks. The banks are numbered 0 through 7 in each CSU of models 172 through 174. In model 175, which always contains CSU-0 and CSU-1, the banks are numbered 0 through 15. The number of words contained in a CM bank depends on the CM size which is determined by the number of quadrants within each CSU.

A quadrant is a division of CM that contains eight CM banks in CSU-0. When CSU-1 is used, the quadrant includes the additional CM banks in that unit. Up to three quadrants may be added to increase any of the basic CM sizes. The addition of quadrants causes the words per CM bank to increase. For example, the words per bank in model 172 increase from 4096 to 16,384 with the addition of quadrants 1 through 3. A special application of quadrant 1 in models 172 and 175 permits a CM size to be increased without the addition of a complete quadrant. Quadrants are added with plug-in CM modules that contain semiconductor memory chips.

The CMs have phased addressing which consists of a sequential bank addressing and sequential word addressing. Sequential address references from CMC to the CMs may occur every 50 nanoseconds (maximum rate). This rate and a CM cycle time of 400 nanoseconds permit up to eight CM banks to be active at any one time. Each CM bank has an access time of 400 nanoseconds at the CSU chassis ports and a maximum data transfer rate of one word every 50 nanoseconds.

The advantage of this high degree of memory interleaving is that a high transfer rate is achieved, much higher than to be expected from just the cycle time of the memory. Furthermore, the architecture of the CDC CYBER 170 requires multiple parallel access to central memory.

TABLE 2-6. MODELS 172 THROUGH 174 CENTRAL MEMORY SIZES

System Model	CM Size (Words)	Words Per Bank	CSU-0 Memory Banks 0 1 2 3 4 5 6 7	CSU-1 Memory Banks 0 1 2 3 4 5 6 7
172	32,768	4,096	Quadrant 0	
172	49,152	6,144	Quadrant 0 Quadrant 1	
172 173 174	65,536	8,192	Quadrant 0 Quadrant 1	
172 173 174	98,304	12,288	Quadrant 0 Quadrant 1 Quadrant 2	
172 173 174	131,072	16,384	Quadrant 0 Quadrant 1 Quadrant 2 Quadrant 3	
173 174	196,608	16,384 in CSU-0 8,192 in CSU-1	Quadrant 0 Quadrant 1	Quadrant 2 Quadrant 3
173 174	262,144	16,384	Quadrant 0 Quadrant 1	Quadrant 2 Quadrant 3

TABLE 2-7. MODEL 175 CENTRAL MEMORY SIZES

System Model	CM Size (Words)	Words Per Bank	CSU-0 Memory Banks 0 1 2 3 4 5 6 7	CSU-1 Memory Banks 8 9 10 11 12 13 14 15
175	65,536	4,096	Quadrant 0	
175	98,304	6,144	Quadrant 0 Quadrant 1	
175	131,072	8,192	Quadrant 0 Quadrant 1	
175	196,608	12,288	Quadrant 0 Quadrant 1 Quadrant 2	
175	262,144	16,384	Quadrant 0 Quadrant 1 Quadrant 2 Quadrant 3	

ADDRESS FORMAT

The location of each word in CM is identified by an 18-bit address in CMC. The format for the address and a resulting CSU address format for models 172 through 174 are shown in Figure 2-10, and for model 175 in Figure 2-11. The two CMC address formats differ because of addressing requirements within the models. The differences exist in the location of the CSU SEL bit. In models 172 through 174, the bit is in position 17. In model 175, the bit is in position 3. Each CMC address format provides 14 bits for the CSU address format. This format is the same in all models.

The CMC address format bits address one CSU word by first selecting CSU-0 or CSU-1 with the CSU SEL bit and one of the eight CM banks within the selected CSU with the BANK SEL bits. The CM word is further addressed by the QUAD SEL bits which select one of four quadrants, narrowing the word selection to one bank and one quadrant. The CHIP SEL bits select one of four columns of semiconductor memory chips on the CM modules in the selected bank and quadrant. At this point, 68 memory chips are selected. Each chip is capable of storing 1024 bits. One bit is selected from each of the 68 chips by the CELL ADDRESS bits to complete the addressing of one 68-bit word.

CSU FORMAT

PAR BIT	QUAD SEL	CELL ADDRESS	CHIP SEL

CMC FORMAT

PAR BIT	CSU SEL	QUAD SEL	CELL ADDRESS	CHIP SEL	BANK SEL

18   17   16 15 14   5 4   3 2   0
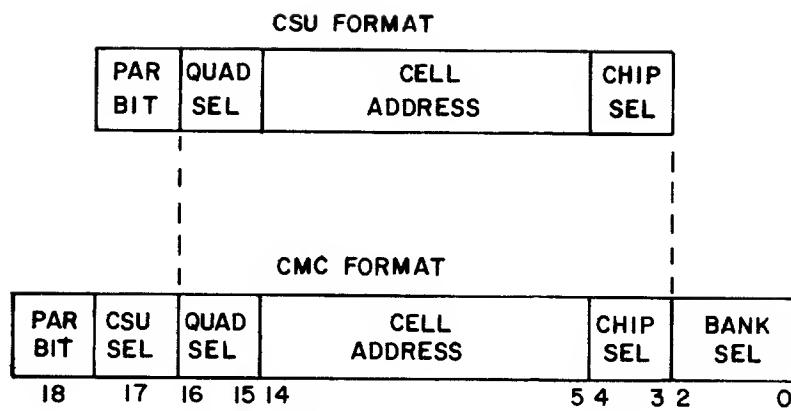
Figure 2-10.   Models 172 through 174 CM Address Formats

CSU FORMAT

PAR BIT	QUAD SEL	CELL ADDRESS	CHIP SEL

CMC FORMAT

PAR BIT	QUAD SEL	CELL ADDRESS	CHIP SEL	BANK SEL

18   17   16 15   6 5   4 3   0
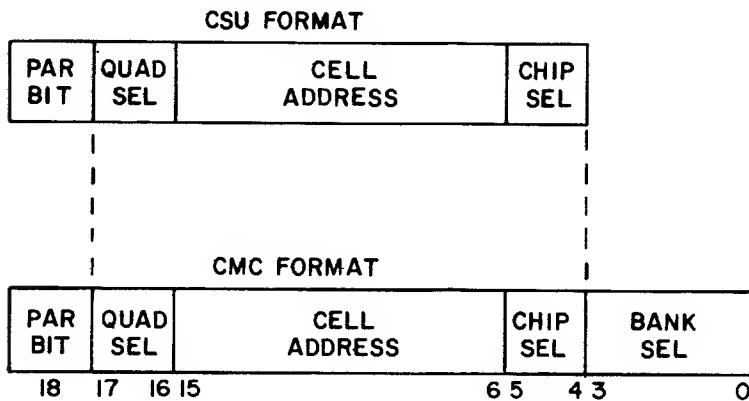
Figure 2-11.   Model 175 CM Address Formats

ADDRESS PARITY

CM accepts the 14-bit address from CMC with 1 parity bit.   Address parity is checked and an error signal is sent to CMC if a parity error is detected.   If the address parity error occurs, a write operation is blocked within CM to protect memory, and a read operation is blocked (returning all ones) to maintain user security.

CENTRAL MEMORY REFERENCE OPERATIONS

Three major operations of CM are read, write, and refresh. These operations are under CMC control.

During a read or write CM reference, CMC sends the address information to CM. The CM sends the address information to all banks. A go bank signal from CMC, decoded from the bank select code, is sent to one of the banks. Only the bank receiving the go bank signal gates the address and data (write operation) into holding registers. The holding registers then select the storage locations and place the data into CM. During a read operation, the addressing is the same except that the absence of a write signal causes data to be read from the addressed location and sent to a common dataout register for transmission to CMC.

CM refresh is, in effect, a CM read operation. A refresh fully restores capacitive charges to storage-bit cells within the semiconductor memory chips of CM. The chips need to be refreshed because they tend to lose capacitive charges that determine whether ones or zeros are stored in the chips. To recharge the chips, CMC sends a go refresh signal to each bank of CM every 25.6 microseconds, providing that an ECS transfer or an exchange jump is not in progress. Each go refresh signal initiates a 400-nanosecond refresh cycle. Each refresh cycle accesses one-fourth of the entire CM. Each memory chip requires 32 refresh cycles (32 addresses) to completely refresh the chip. Therefore, refreshing the entire CM requires 128 (4 times 32) refresh cycles. With the refresh cycles occurring every 25.6 microseconds, the entire CM can be refreshed every 3.2768 milliseconds.

During an ECS block transfer, a refresh cycle cannot be started for all the banks at the same time without affecting the ECS transfer. To avoid degradation of ECS transfer rate, the go refresh signal is issued selectively to a phased bank which would not be referenced for the next 400 nanoseconds during the ECS block transfer.

CM refresh waits for an exchange jump to complete before initiating one of the cycles.

CENTRAL MEMORY RECONFIGURATION

Central memory reconfiguration is a manually performed function that permits the computer operator to restructure the CM addresses so that a failing part of CM can be quickly locked out to provide a continuous block of usable CM. CM reconfiguration is accomplished by setting switches to manipulate upper address bits. Hardware configures the CM quadrants so that sequential addressing is maintained. Reconfiguration options for the four models are:

Model 172	131K to 98K to 65K to 32K and 49K to 32K
Model 173	262K to 196K to 131K to 98K to 65K
Model 174	262K to 196K to 131K to 98K to 65K
Model 175	262K to 196K to 131K to 65K and 98K to 65K (only if 32K portion fails)

A reconfiguration permits only one part of the CM to be locked out at a time. The reconfiguration provides the same-sequential addressing characteristics as a same-size normally operating CM without reconfiguration.

REFRESH FAULT

Each CSU checks for a refresh fault caused by constant refresh or a refresh which may occur too often and cause excessive power dissipation. Upon detection of a refresh fault, a CM disable flip-flop sets and prevents any request or refresh access to CM. Until the CM disable flip-flop clears, the CSU returns all ones on a CM read. A CSU fault status bit sets in the status and control register. A master clear is required to clear the CM disabled flip-flops. While the CM disable flip-flop is set, CM cannot be refreshed; therefore, data is no longer valid and must be reloaded after the fault condition is cleared.

PERIPHERAL PROCESSOR SUBSYSTEM

The PPS consists of 10 peripheral processors (PPs). Each PP is a functionally independent computer with a memory and a repertoire of 64 instructions. The PPs share access to CM and 12 bidirectional I/O channels. The PPs are organized in a multiplexing system, termed barrel and slot, which allows them to share common hardware for arithmetic, logical, and I/O operations without losing speed or independence.

The PPS can be expanded to 14, 17, or 20 PPs in system models 173 through 175. The expansion is accomplished by adding a second PPS chassis to the mainframe and always includes an expansion of 12 additional I/O channels. Any of the PPs can access any of the I/O channels.

The PPS operates in a 1000-nanosecond (1X mode) major cycle time for CDC CYBER 70 software compatibility or in a 500-nanosecond (2X mode) major cycle time. The major cycle time is selectable with bit 84 of the status and control register. All PPs communicate with either external equipment or each other over the 12 or 24 independent (12 bits plus 1 parity bit) bidirectional I/O channels. Only one piece of external equipment can communicate over one channel at a time, but all channels can be active at the same time.

Channel instructions direct all activities with external equipment. These instructions are used to select any equipment on any channel and transfer data to or from the selected equipment.

Each PP exchanges data with CM through CMC in 60-bit words. In a write operation, five successive 12-bit PP words are assembled into a 60-bit word and sent to CMC. In a read operation, a 60-bit word from CM is disassembled into five 12-bit words and sent to successive locations in the peripheral processor memory (PPM). Separate assembly read and write paths to CM are time-shared by each of the 10 PPs. Assembly/disassembly registers are called pyramids. These pyramids are also provided for the 4, 7, or 10 PPs in the second PPS chassis.

Data transmission parity is generated on all CM writes and sent to CMC. Data transmission parity is checked on all CM reads. If a data parity error is detected, a bit is in the status and control register.

DEADSTART

Deadstart is a PPS operation that provides initial starting of the computer, dumping of the contents of peripheral and control processor memories to an output device (normally a printer), or sweeping PPMs without executing instructions. Deadstart is controlled by the deadstart panel in bay 1. The panel includes controls for selecting any PP as logical PP-0 (control PP). Another control enables central exchange jump/monitor exchange jump (CEJ/MEJ).

PERIPHERAL PROCESSOR MEMORY

Each PP has an independent 4096-word, 13-bit (12 data bits plus 1 parity bit) metal-oxide semiconductor (MOS) memory.

PPM data words are checked for parity on each read. If a parity error is detected, a bit is set in the status and control register. All PPs of a PPS can be selected to stop on PPM parity error by setting bit 95 in the status and control register.

A PPM reconfiguration feature permits the user to restore the PPS operation after a critical failure of a PPM designated as PPM-0. PPM-0 has a special controlling function at dead-start time. The reconfiguration is accomplished by logically exchanging the failing PPM with a good PPM and degrading the PPS to operate without the failing PPM. Logical selection of PPM-0 is performed by setting switches on the deadstart panel. Degrading the PPS must be done through the operating system. The reconfiguration permits computer operation to continue without the failing PPM so that the failing PPM can be corrected during scheduled maintenance.

The PPMs use the same memory chips as CM and also require refreshing. Refreshing occurs once every 32 microseconds and requires a period of 500 nanoseconds. During PPS operation at a 1X speed, the refresh cycle is invisible to PP operations. At a 2X speed, all PPM references are locked out during a refresh cycle.

BARREL AND SLOT

The 10 PPs are combined in a multiplexing arrangement termed barrel and slot (Figure 2-12). This arrangement allows the accumulator (A), program address (P), auxiliary accumulator (Q), and translation (K) registers of each PP to time-share common instruction-control hardware. The hardware-sharing permits logical, I/O, and other PP operations to occur without sacrificing speed or independence of the individual PPs. The barrel and slot arrangement includes common data paths to and from CM and to and from 12 I/O channels.

The barrel is a matrix of flip-flops that holds the current instruction and operand for each of nine PPs, while the slot contains the current instruction and operand for the tenth PP. The barrel gives each PP a turn at using the common instruction-control hardware in the slot by shifting the quantities around the barrel from the slot output to the slot input.

Each time data enters the slot, a portion of the instruction for that data is executed. The slot performs tasks such as arithmetic and logic operations and program address manipulation. Complete execution of an instruction may require the A, P, Q, and K register quantities to go more than one trip around the barrel and through the slot.

TEN PERIPHERAL PROCESSOR MEMORIES

Figure 2-12. Barrel and Slot Operation
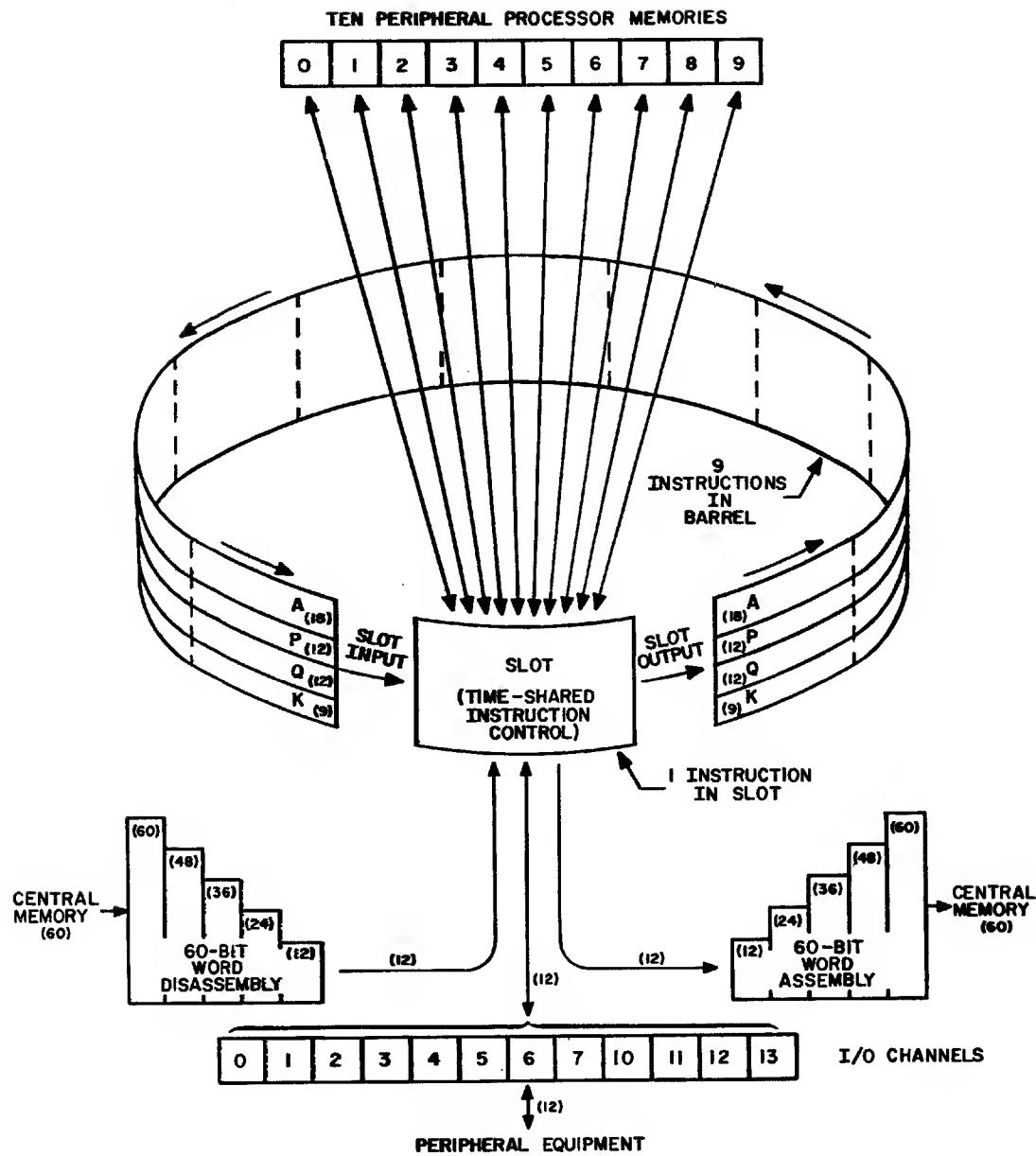
NOTE:
NUMBERS IN PARENTHESES ARE BIT QUANTITIES.

The barrel and slot operation provides PP program operating speeds of 1X and 2X. These speeds are program-selectable by a single bit in the status and control register. When cleared, the bit causes the PPs to operate at 1X speed that consists of a 50-nanosecond slot time for each PP once every 1000 nanoseconds. When set, the bit causes the PPs to operate at 2X speed that consists of a 50-nanosecond slot time for each PP once every 500 nanoseconds.

The PPM may be referenced once each time the PP passes around the barrel and through the slot. During its slot time, the PP may also communicate in 12-bit quantities with CM or with any of the I/O channels except during a CM refresh cycle.

The 12-bit quantities that go to CM are assembled into 60-bit words before being transferred. Similarly, the 60-bit words from CM are disassembled into 12-bit quantities prior to use in the barrel and slot.

The PPMs are numbered 0 through 9. PPS SELECT switches on the deadstart panel permit any one of the PPMs to be selected as PPM-0. Following a PPM-0 selection, the 10 PPMs remain in order with new but consecutive numbers that follow PPM-0.

For example, if PPM-8 is selected as PPM-0, then PPM-9 becomes PPM-1 and the original PPM-0 becomes PPM-2. Since each PPM is associated with a PP, the same numbering scheme applies to the PPs; only the PP numbering changes. The PPs retain the same positions in the barrel.

INPUT/OUTPUT

Any PP can access any of the 12 bidirectional I/O channels of a PPS or any of the 24 bidirectional channels of an expanded system. All PPs communicate with external equipment and each other through the independent I/O channels. Each channel may be connected to one or more pieces of external equipment, but only one piece of equipment can use a channel at one time. All channels can be active simultaneously.

Each I/O channel transfers a 12-bit word plus 1 parity bit at rates up to one word every microsecond when the PPs are operating at 1X speed. When the PPs operate at 2X speed, channel transfers occur at a rate up to one word every 500 nanoseconds with one exception. This exception occurs only in a 14-, 17-, or 20-PP system.

Pulse communication is used on all data and control lines of a channel. All control lines are synchronized to the PP clock system.

An unanswered I/O or CM request from a PP causes the PP to hang, causing the PP to operate in a loop. The loop makes the PP continually look for a reply, keeping the PP from proceeding to other operations. The PP may be released from the hung condition by a dead-start, or if CM was the cause, by a control bit in the status and control register.

Parity is generated on the output channels and is checked on the input channels. If a parity error is detected on input data transfer, a bit is set in the status and control register. The status and control register channel parity error status bits are not set on output data transfer parity errors. Each channel is provided with a switch to disable checking parity on input data from external devices that have no parity capability.

Data flows between a PPM and the external device in blocks of words. A block may be as small as one word. A single word may be transferred between an external device and a PP A register.

STATUS AND CONTROL REGISTER

A status and control register is included in the peripheral processor subsystem primarily as a maintenance aid. This register monitors error conditions that might occur including address and data parity errors and SECDED conditions which include address information. The register is program-controlled. Visual light displays are included on all status bits. For a detailed description of each of the status and control bits of the register, refer to the CDC CYBER 170 Computer Systems Hardware Reference Manual, publication number 60420000.

REAL-TIME CLOCK

The computing system contains a real-time clock. The clock may be used to determine program running time, as a reference to track the time-of-day, or for other functions determined by the computer programs.

The clock runs continuously during computer power application. Output from the clock comes from a 12-bit register that increments once every microsecond to the maximum capacity of the register (4096 microseconds). When the register reaches capacity, it resets and continues counting. The counting cannot be preset or altered.

Any of the PPs may read the 12-bit clock output with the input to A channel d, 70 instruction. The instruction permits access to the clock on internal channel 14 (octal). Any attempts to output information on channel 14 cause it to hang.

DATA CHANNEL CONVERTERS

The data channel converters (DCCs) are parity enhanced interfaces that extend the types of peripheral equipment used with the CDC CYBER 170 Series Computer Systems. In the basic computer systems, two DCCs are contained in the PPS-0 chassis. In an expanded system, two additional DCCs may be optionally installed in the PPS-1 chassis.

Each DCC is assigned to one I/O channel and may share the channel with up to seven peripheral units such as: a magnetic tape controller, a console display controller, or other DCCs.

DISPLAY CONTROLLER

The controller provides digital and analog information for alphanumeric presentations on a display station screen, and receives digital information from a keyboard on the display station. All operations are under program control of the PPs. The display controller is contained in the standard PPS-0 chassis. Connections to an optional second display station are available at the controller.

DISPLAY STATION

The CDC CYBER 170 Display Station provides a visual, alphanumeric readout for the computer. The receipt of symbol and position information from the computer enables displaying program information on a console 21-inch cathode-ray tube (CRT). The station also contains an alphanumeric keyboard which enables an operator to send data to the computer. The keyboard and CRT combination permits the computer operator to modify computer programs and view the result on the screen. The computer outputs two alternate, nonrelated data streams. The display station keyboard has a switch which enables the operator to select either of the data streams or to select both for presentation on the CRT.

CONDENSING UNIT

A 3-ton condensing unit provides conduction cooling for each bay of models 172 through 174. The condensing unit mounts within the bay(s) as shown in Figures 2-5 through 2-7. A separate stand-alone 10-ton condensing unit provides the cooling for the model 175. Each condensing unit cools the mainframe chassis by pumping refrigerant through chassis cold bars mounted adjacent to the logic and memory modules.

EXTENDED CORE STORAGE SUBSYSTEM

The CDC CYBER 170 Extended Core Storage (ECS) Subsystem is an optional on-line, random-access, magnetic-core memory system which augments CM. The subsystem has a fixed-word length and is capable of two-way communication between its memory banks and the mainframe.

High transfer rates and short access times of ECS make it ideal for use as an I/O buffer between CM and rotating mass storage devices, as a high-speed program swapping device, as a storage device for large data arrays, as a storage device for frequently used programs, such as system and PP routines, and as a communications device for multimainframe systems.

ECS is available in sizes ranging from 131,072 60-bit words (one bank) to 2,097,152 60-bit words (16 banks). Some words are kept in reserve in each bank for degradation purposes.

Configuration of the ECS subsystem (Figures 2-1 through 2-4) includes an ECS coupler, an ECS controller, ECS memory banks, and a distributive data path.

ECS COUPLER

The ECS coupler physically mounts within the mainframe cabinet. The coupler interfaces the mainframe with the ECS subsystem through the ECS controller.

During a block transfer operation, the ECS coupler must request the ECS controller every 800 nanoseconds to maintain the maximum rate of one 60-bit word every 100 nanoseconds. This gives a maximum transfer rate of 600 million bits every second.

ECS CONTROLLER

The ECS controller regulates access and data transfers to and from the ECS memory banks. The controller has four access channels and one ECS interface. Each access channel connects to one ECS coupler or distributive data path and carries 60 data bits plus 1 parity bit. The ECS interface carries 480 data bits plus 8 parity bits. The controller performs time-sharing on the four access channels, and assembles/disassembles 60-bit/480-bit words during data transfers. Data parity is generated and checked on the access channels and ECS interface. The ECS controller also has:

- A capability of checking address parity

- A capability of switching 262K and larger systems to 50 percent capacity

- A flag register which software can use to coordinate ECS references

ECS MEMORY BANKS

Extended core storage contains 1, 2, 4, 8, or 16 memory banks, each capable of storing 131,072 60-bit words. A cabinet (bay) holds up to four memory banks. Each ECS bank address stores one ECS record. An ECS record contains 8 words, each consisting of 60 data bits plus 1 parity bit. References as low as one 60-bit word are possible.

An ECS subsystem must have four or more 131K-word memory banks to achieve a transfer rate of one 60-bit word each 100 nanoseconds. If a subsystem has four or more banks, the ECS controller staggers ECS references so that one bank is referenced while the previously referenced bank is recovering, and so on. If ECS has two 131K-word banks, the ECS controller allows two sequential requests. A third request must wait until a bank becomes free. Thus, 60-bit words transfer in a pattern of one word every 100 nanoseconds for 1600 nanoseconds, wait 1600 nanoseconds, transfer another 16 words, and so on. This gives an effective rate of one word every 200 nanoseconds. If the system has one 131K-word bank, the ECS controller allows a second request only after the first memory cycle is complete. Sixty-bit words transfer in a pattern of one word every 100 nanoseconds for 800 nanoseconds, wait 2400 nanoseconds, and so on. The effective transfer rate is one word every 400 nanoseconds.

DISTRIBUTIVE DATA PATH

The distributive data path provides a path of data flow between ECS and the PPs. The path allows fast PP access to data in ECS using an I/O channel, and greatly reduces the data transfers through CM. This allows other system components such as PPs or a CP to access CM more frequently and makes ECS an almost ideal device to store successively used PP routines and other PP-driven system programs.

The distributive data path consists of one to four 480-bit buffer registers. Each register connects to a standard I/O channel for maximum overlap of data transfer. All four registers share a single access to ECS. This arrangement allows up to four PPs to transfer data simultaneously to ECS at the maximum channel rate. A 480-bit ECS word is assembled from a 40-word PP block in about 43 microseconds.

SYSTEM CONFIGURATIONS

The CDC CYBER 170 Computer Systems are available in a number of configurations to satisfy the particular needs of individual users. Most of the system upgrades are available as field installations. This offers each user excellent growth capabilities, optimization of investments, and minimization of business interruptions. System upgrades create the configurations shown in Figures 3-1 through 3-4. The following paragraphs add further explanations of system alternatives.

CENTRAL PROCESSOR UPGRADES

The system performance may be increased by field-upgrading the CP of the model 172 to a model 173, or by upgrading the CP of the model 173 to a model 174 as follows:

- 172 plus 10316-1 gives 173-X
- 173 plus 10316-2 gives 174-X

The upgrading of a model 172, 173, or 174 to a model 175 requires replacement of the mainframe.

CENTRAL MEMORY UPGRADES

The CM upgrades are as follows:

- Model 172 Upgrade

  172-2 plus 10312-3 gives 172-3
  172-3 plus 10312-4 gives 172-4
  172-4 plus 10312-6 gives 172-6
  172-6 plus 10312-8 gives 172-8

- Model 173 Upgrade (10317-1 cabinet and power expansion may be required)

  173-4 plus 10312-6 gives 173-6
  173-6 plus 10312-8 gives 173-8
  173-8 plus 10312-12 gives 173-12
  173-12 plus 10312-16 gives 173-16

- Model 174 Upgrade

  174-4 plus 10312-6 gives 174-6
  174-6 plus 10312-8 gives 174-8
  174-8 plus 10312-12 gives 174-12
  174-12 plus 10312-16 gives 174-16

- Model 175 Upgrade (10317 cabinet and power expansion may be required)

  175-4 plus 10313-6 gives 175-6
  175-6 plus 10313-8 gives 175-8
  175-8 plus 10313-12 gives 175-12
  175-12 plus 10313-16 gives 175-16

# PERIPHERAL PROCESSOR AND INPUT/OUTPUT CHANNEL UPGRADES

The configuration of model 172 and the basic configurations of models 173 through 175 contain 10 PPs and 12 I/O channels. Upgrading of the PPs and I/O channels for models 173 through 175 may be achieved as follows:

- Model 173 and 174 Upgrade

  10314-1 Adds 4 PPs and 12 I/O channels to a 10 PP, 12 I/O channel system
  10314-2 Adds 3 PPs to a 14 PP, 24 I/O channel system
  10314-2 Adds 3 PPs to a 17 PP, 24 I/O channel system

- Model 175 Upgrade

  10314-51 Adds 4 PPs and 12 I/O channels to a 10 PP, 12 I/O channel system
  10314-52 Adds 3 PPs to a 14 PP, 24 I/O channel system
  10314-52 Adds 3 PPs to a 17 PP, 24 I/O channel system

EXTENDED CORE STORAGE UPGRADES

The basic ECS subsystem (7030-X) is upgraded by addition of storage increments as follows:

| Model	ECS Words	
7030-1	125K	plus 10271-1 gives 7030-2
7030-2	250K	plus 10271-2 gives 7030-4
7030-4	500K	plus 10271-4 gives 7030-8
7030-8	1M	plus 10271-8 gives 7030-16
7030-16	2M	
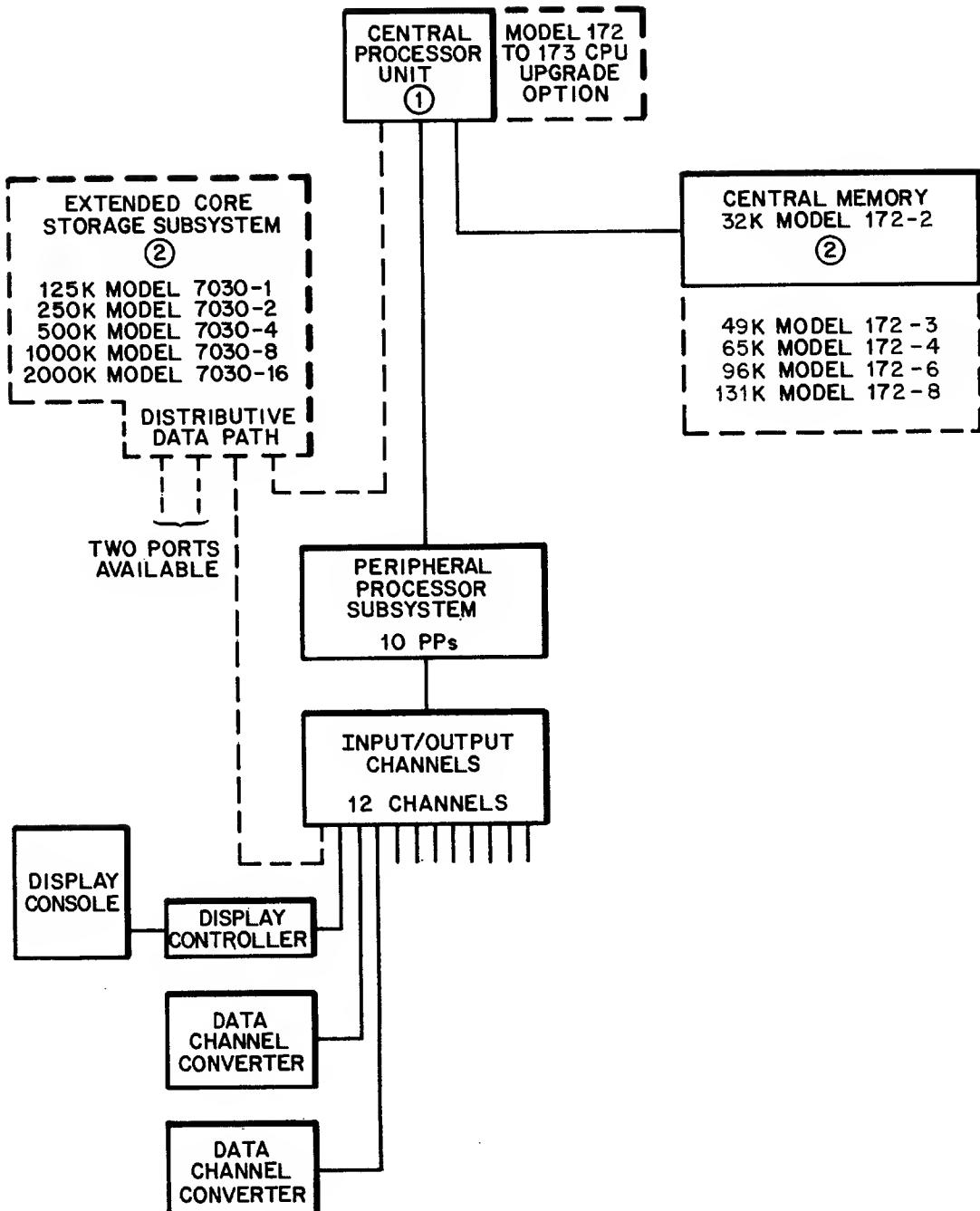
Figure 3-1. Model 172 System Upgrades
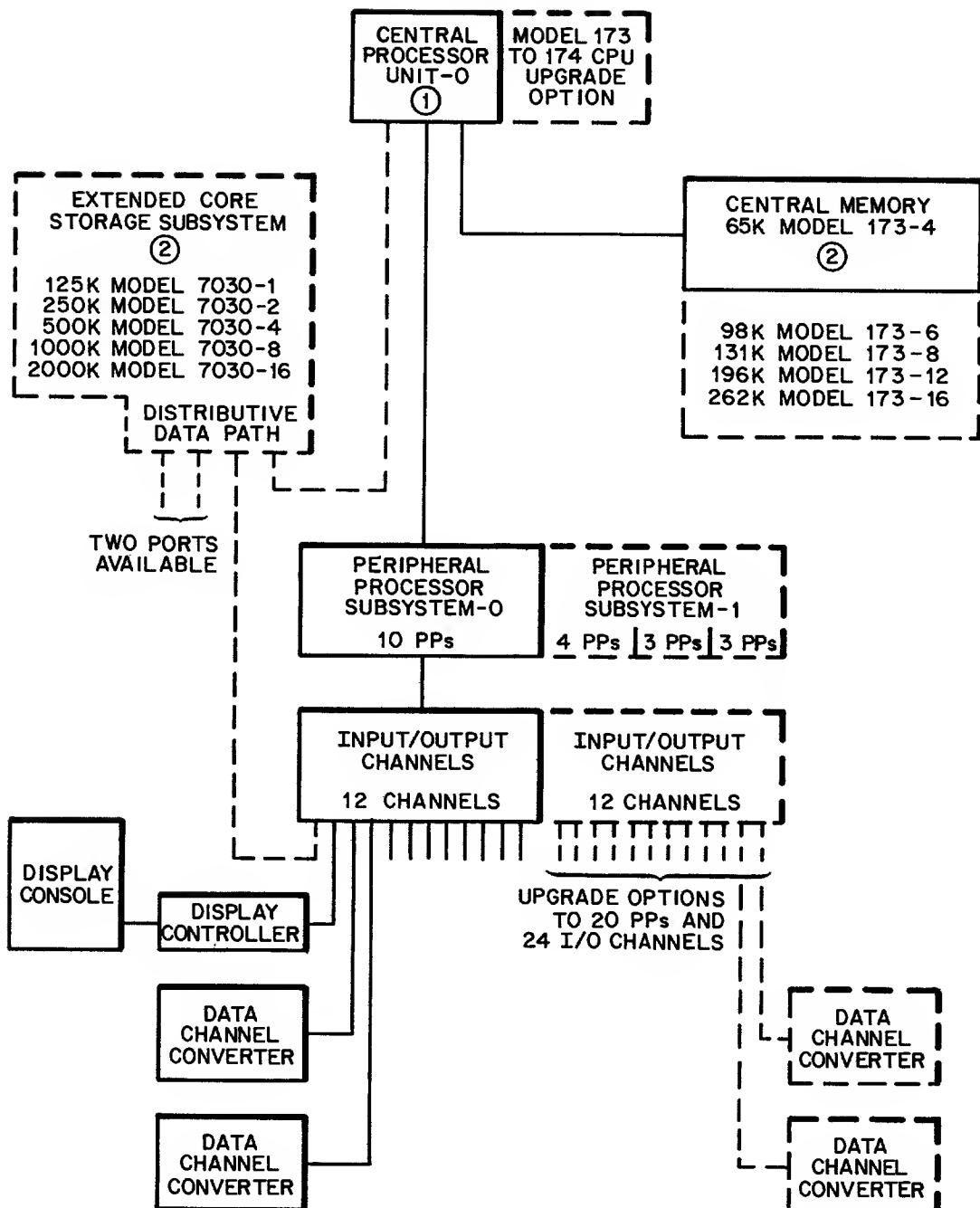
NOTES:

① UNIFIED CPU WITH COMPARE/MOVE UNIT.

② EACH BASIC MODEL HAS THE OPTION OF BEING UPGRADED TO THE STORAGE CAPACITY OF THE NEXT MODEL.

Figure 3-2. Model 173 System Upgrades

The diagram contains the following labeled blocks and text:

CENTRAL PROCESSOR UNIT-0 ①

MODEL 173 TO 174 CPU UPGRADE OPTION

EXTENDED CORE STORAGE SUBSYSTEM ②

125K MODEL 7030-1
250K MODEL 7030-2
500K MODEL 7030-4
1000K MODEL 7030-8
2000K MODEL 7030-16

DISTRIBUTIVE DATA PATH

CENTRAL MEMORY 65K MODEL 173-4 ②

98K MODEL 173-6
131K MODEL 173-8
196K MODEL 173-12
262K MODEL 173-16

TWO PORTS AVAILABLE

PERIPHERAL PROCESSOR SUBSYSTEM-0
10 PPs

PERIPHERAL PROCESSOR SUBSYSTEM-1
4 PPs | 3 PPs | 3 PPs

INPUT/OUTPUT CHANNELS
12 CHANNELS

INPUT/OUTPUT CHANNELS
12 CHANNELS

UPGRADE OPTIONS TO 20 PPs AND 24 I/O CHANNELS

DISPLAY CONSOLE

DISPLAY CONTROLLER

DATA CHANNEL CONVERTER

DATA CHANNEL CONVERTER

DATA CHANNEL CONVERTER

DATA CHANNEL CONVERTER

NOTES:

① UNIFIED CPU WITH COMPARE/MOVE UNIT.

② EACH BASIC MODEL HAS THE OPTION OF BEING UPGRADED TO THE STORAGE CAPACITY OF THE NEXT MODEL.

NOTES:

① UNIFIED CPU WITH COMPARE/MOVE UNIT.

② EACH BASIC MODEL HAS THE OPTION OF BEING UPGRADED TO THE STORAGE CAPACITY OF THE NEXT MODEL.

Figure 3-3. Model 174 System Upgrades

CENTRAL
PROCESSOR
UNIT-0
①

EXTENDED CORE
STORAGE SUBSYSTEM
②

125K MODEL 7030-1
250K MODEL 7030-2
500K MODEL 7030-4
1000K MODEL 7030-8
2000K MODEL 7030-16

DISTRIBUTIVE
DATA PATH

CENTRAL MEMORY
65K MODEL 173-4
②

98K MODEL 173-6
131K MODEL 173-8
196K MODEL 173-12
262K MODEL 173-16

TWO PORTS
AVAILABLE

PERIPHERAL
PROCESSOR
SUBSYSTEM-0
10 PPs

PERIPHERAL
PROCESSOR
SUBSYSTEM-1
4 PPs | 3 PPs | 3 PPs

INPUT/OUTPUT
CHANNELS
12 CHANNELS

INPUT/OUTPUT
CHANNELS
12 CHANNELS

DISPLAY
CONSOLE

DISPLAY
CONTROLLER

UPGRADE OPTIONS
TO 20 PPs AND
24 I/O CHANNELS

DATA
CHANNEL
CONVERTER

DATA
CHANNEL
CONVERTER

DATA
CHANNEL
CONVERTER

DATA
CHANNEL
CONVERTER

NOTES:

① MULTIFUNCTION CPU.

② EACH BASIC MODEL HAS THE OPTION OF BEING UPGRADED TO
THE STORAGE CAPACITY OF THE NEXT MODEL.

Figure 3-4.   Model 175 System Upgrades

The CDC CYBER 170 systems accommodate a variety of CDC peripheral equipment as shown in Table 4-1. Figures 4-1 through 4-3 show how to configure frequently used peripheral equipment with CDC CYBER 170 systems.

TABLE 4-1. PERIPHERAL EQUIPMENT

Product No.	Description	Product No.	Description
350	Paper Tape Reader	3270	Transfer Switch Controller
405	Card Reader	3398	Digigraphics Controller
415	Card Punch	3423	Magnetic Tape Controller
415-30	Card Punch and Controller	3446	Card Punch Controller
501	Line Printer	3447	Card Reader Controller
505	Line Printer	3518	Magnetic Tape Controller
512	Line Printer	3528	Magnetic Tape Controller
580-12, 16, 20	Train Printer Subsystem	3553	Mass Storage Controller
60X	Magnetic Tape Transport	3555	Line Printer Controller
657	Magnetic Tape Transport	3691	Paper Tape Reader Punch
66X	Magnetic Tape Transport	6638	Disk System
711	CRT Display Transport	6640	ECS Storage Controller
713-10	Conversational Display Terminal	6642	Distributive Data Path
734	Batch Terminal Controller	6671	Data Set Controller
841	Multiple Disk Drive Module	6673	Data Set Controller
844-21	Disk Storage Unit	6674	Data Set Controller
844-41	Disk Storage Unit	6676	Data Set Controller
853	Disk Storage Drive	6681	Data Channel Converter
2550	Host Communications Processor	6683	Satellite Coupler
2550-100	Emulation 6671/6676	7021	Magnetic Tape Controller
3228	Magnetic Tape Controller	7030	CDC CYBER 70 Extended Core Storage
3229	Magnetic Tape Controller	7054	Mass Storage Controller
3256	Line Printer Controller	8271	Transfer Switch
		10329	Manual Multi-Controller Switch
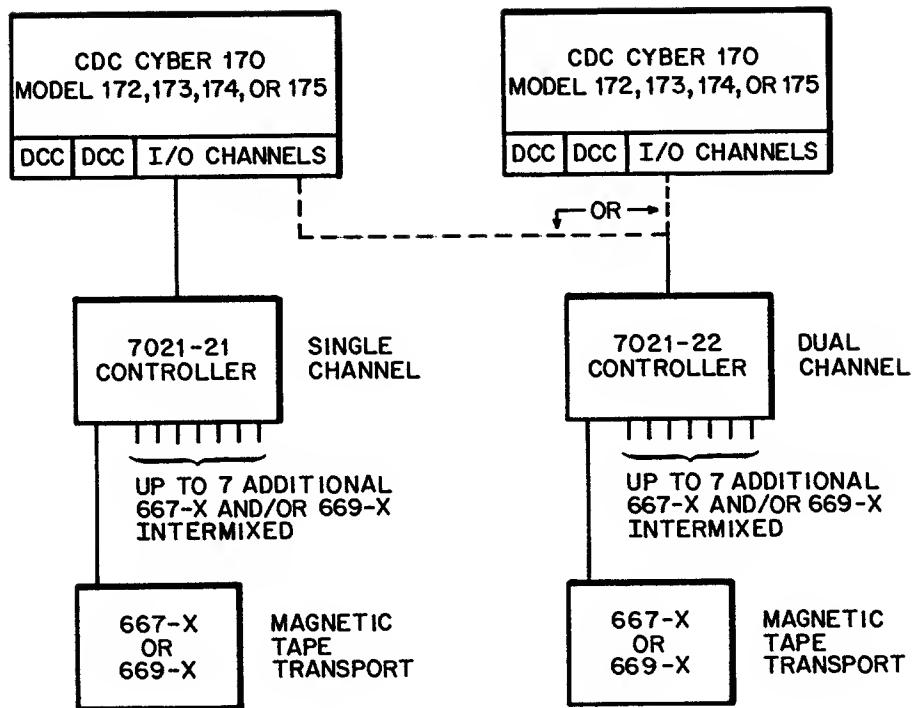
NOTES:
1. TWO DATA CHANNEL CONVERTERS (DCC'S) ARE INCLUDED WITH EACH BASIC SYSTEM.
2. DASHED LINES INDICATE OPTIONAL CONNECTIONS.
3. 667-X: 667-2, 667-3, 667-4 (SEVEN-TRACK).
4. 669-X: 669-2, 669-3, 669-4 (NINE-TRACK).
5. 7021-2X: 7021-21 SINGLE CHANNEL, 7021-22 DUAL CHANNEL.

Figure 4-1. Magnetic Tape (667-X/669-X) Storage
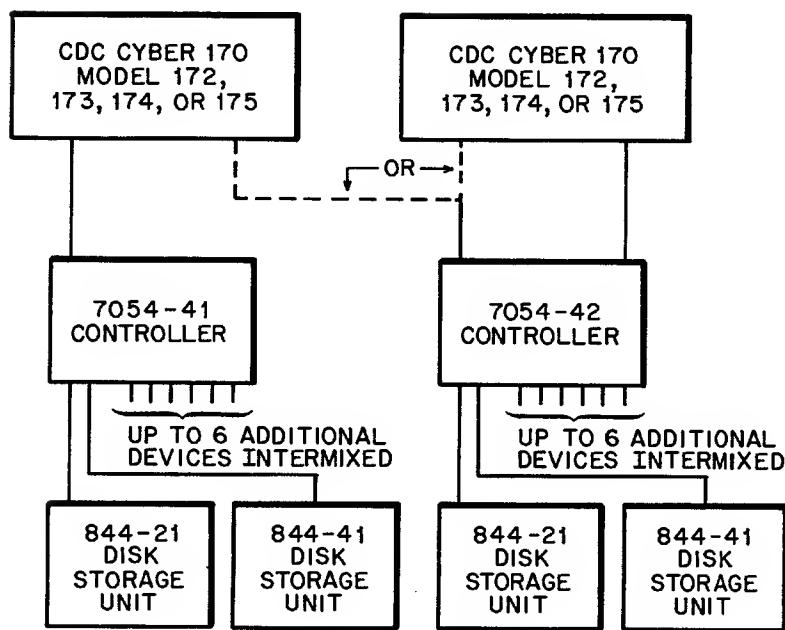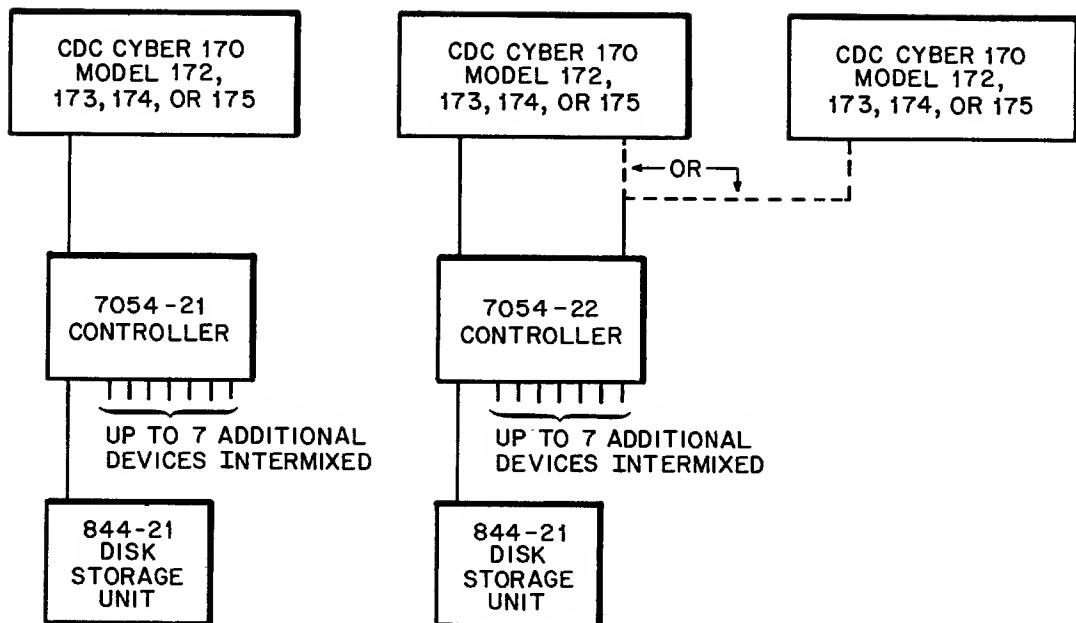
NOTE:

A 10339-1 OPTION CONVERTS A 7054-2X INTO A 7054-4X.

Figure 4-2.   Disk Storage Mass Storage
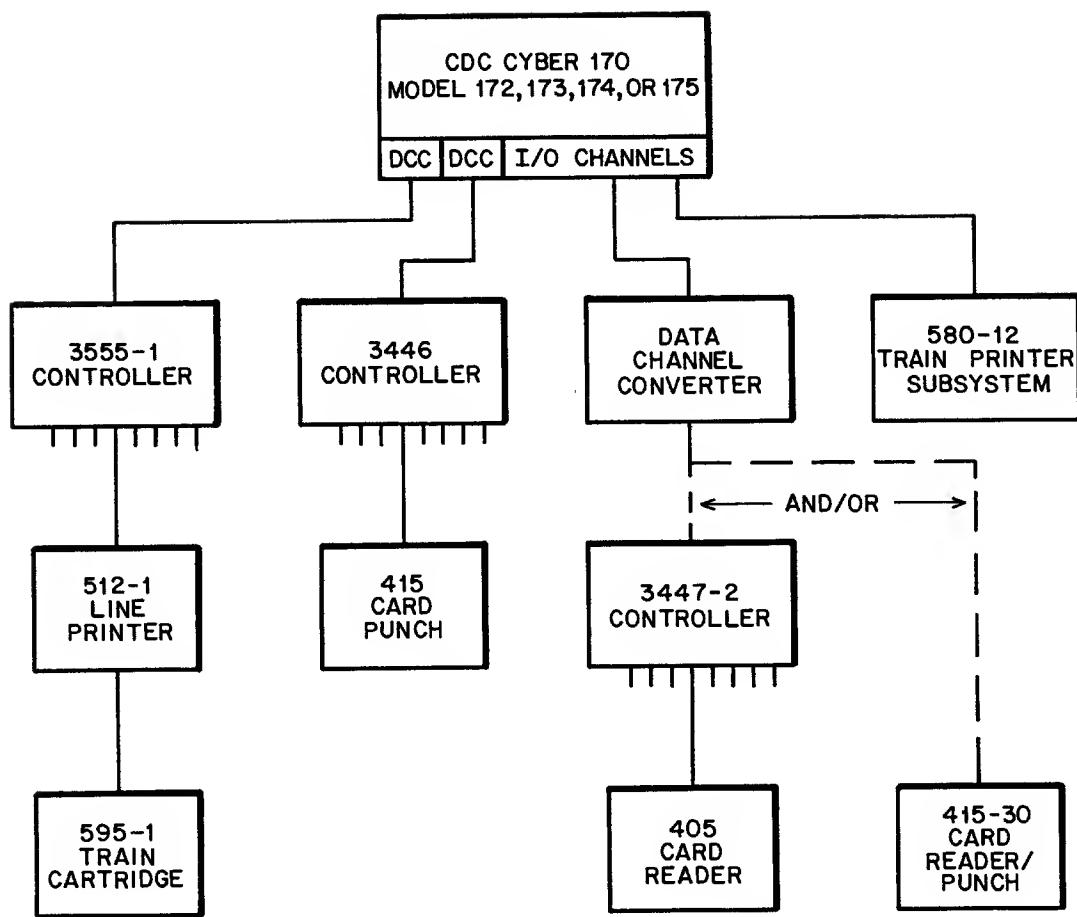
NOTES:

1. THIS FIGURE IS INTENDED TO SHOW EXAMPLES OF WAYS OF CONNECTING PERIPHERAL EQUIPMENT TO A CDC CYBER 170 SYSTEM. ALL RECORD UNIT EQUIPMENT IS USUALLY CONNECTED TO ONE CHANNEL.

2. TWO DATA CHANNEL CONVERTERS (DCC'S) ARE INCLUDED WITH EACH BASIC SYSTEM.

3. DASHED LINES INDICATE OPTIONAL CONNECTIONS.

Figure 4-3. Local Unit Record Subsystem

HARDWARE MANUALS

The CDC CYBER 170 Hardware manuals are listed in the System Publication Index (Figure 5-1). The index is in the form of a family tree that shows the relationship of the manuals to each other and to the various CDC CYBER 170 systems. The manuals in the index have an eight-digit publication number which must be used when ordering manuals.

GENERAL PROMOTIONAL MATERIAL

CDC CYBER 170 general promotional materials consist of colored brochures. They are identified by a six-digit publication number and are as follows:

Control Data Publication	Publication No.
CDC CYBER 170 Series Applications Guide	200,998
Control Data 2550 Series Host Communications Processor	201,038
CDC CYBER 170 Series/Earmarked for Use	200,998
CDC CYBER Power-Source Protection	201,058
Consider All These Peripheral Advantages Control Data CYBER 170 Computer System	200,999
Network Communications Systems for CDC Computer Systems and Data Networks	201,033
Computer Networks — Network Processing Concepts	201,055
Products of Experience — An Executive Guide to the Control Data CYBER One-Seventy Family of Computer Systems	200,997

PUBLICATION ORDERING

All publications should be ordered from:

Control Data Corporation
Literature and Distribution Services
8100 34th Avenue South, P.O. Box 0
Minneapolis, Minnesota 55440

Prices and latest publication revision levels are available from the Control Data Literature Catalog, publication number 90310500.

CYBER 170
HARDWARE
MANUALS

HARDWARE
MAINTENANCE
MANUALS

SYSTEM
MANUALS

MODEL 172

MODEL 173

MODEL 174

MODEL 175

MODELS 172-174

MODEL 175

CPU THEORY, DIAGRAMS
18881800

CP THEORY, DIAGRAMS
60420300

CYBER 170 HARDWARE REFERENCE
60420000

CSU THEORY, DIAGRAMS
18981900

ECS SUBSYSTEM HARDWARE REFERENCE
60430000

PPS THEORY, DIAGRAMS
19982000

DISPLAY CONSOLE HARDWARE REFERENCE/CE
82978200

OPTIONAL PPS THEORY, DIAGRAMS
19982100

I/O SPECIFICATION
19983600

CMC/ECS COUPLER THEORY, DIAGRAMS
19982200

ECS CPLR THEORY, DIAG, WL
60428800

PRINTED CIRCUITS
19983500

CPU WIRE LISTS
19983000

CPU WIRE LISTS
19982300

CP WIRE LISTS
80420400

SITE PREPARATION-GENERAL
80275100

CSU WIRE LISTS
19982400

SITE PREP-MAINFRAME
19981400

SITE PREP-MAINFRAME
60420100

PPS WIRE LISTS
19982500

SITE PREPARATION-PERIPHERAL EQUIPMENT
60275300

OPTIONAL PPS WIRE LISTS
19983300

CMC/ECS COUPLER WIRE LISTS
19982600

CABLES WIRE LISTS
19983200

CABLES WIRE LISTS
19982700

CABLES WIRE LISTS
19983700

CABLES WIRE LISTS
60420200

POWER DISTRIBUTION AND WARNING SYSTEM
19981500 ①

PWR DISTR AND WARN SYS
60420700 ①

NOTES:
① THIS MANUAL CONTAINS ALL SECTIONS EXCEPT MAINTENANCE, PARTS, AND INSTALLATION AND CHECKOUT.

② THIS MANUAL CONTAINS ALL SECTIONS.

③ THIS MANUAL CONTAINS INFORMATION FOR MAINFRAME AND INCLUDES ALL OPTIONS.

REFRIGERATION SYSTEM
19983800 ②

REFRIG SYS
60427800 ②

INSTALLATION AND CHECKOUT
19981700 ③

INST AND CHECKOUT
60420500 ③

MAINTENANCE, PARTS
19981600 ③

MAINTENANCE, PARTS
60420600 ③

ECS SUBSYSTEM
60404700 (ECS), 60425800 (DDP), 60440500 (CONTROLLER)

M-G SET THEORY, MAINTENANCE, ETC.
60166800 (EM), 60420800 (KATO)

M-G SET DIAGRAMS
60423100 (EM), 60419900 (KATO)

Figure 5-1. System Publication Index

COMMENT SHEET

MANUAL TITLE <u>CDC® CYBER 170 Computer Systems</u>

<u>Systems Hardware Handbook</u>

PUBLICATION NO. <u>60447600</u>   REVISION <u>A</u>

FROM: NAME: _____

BUSINESS
ADDRESS: _____

CONTROL DATA

>>> CUT OUT FOR USE AS LOOSE-LEAF BINDER TITLE TAB

CONTROL DATA
CORPORATION